The Open IP ODM

Intel Rangeley Communications Collateral (RCC) Reference Design Platform

User Manual

Revision: 1.00

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Revision History

Date	Revision	Section	Remarks
06/12/2013	0.01		- Initial Draft
06/24/2013	0.02		- Initial feedback updates
06/26/2013	0.03		- Remove optional wording for battery
07/12/2013	0.04		- Change temperature specification for A-step silicon
09/03/2013	1.0		- Official release

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1 RANGELEY COMMUNICATIONS COLLATERAL REFERENCE DESIGN PLATFORM DESCRIPTION

1.1 Overview

The Rangeley Communications Collateral (RCC) platform is based on the Intel Rangeley SOC. Rangeley is a multi-core (up to 8) Intel Atom based SOC product featuring high levels of I/O integration and an Intel QuickAssist hardware acceleration engine. Rangeley is targeted for the routers and security communications market segment. This platform will demonstrate Rangeley in an embedded, lower power, and small form factor solution. The RCC block diagram is shown in Figure 1.

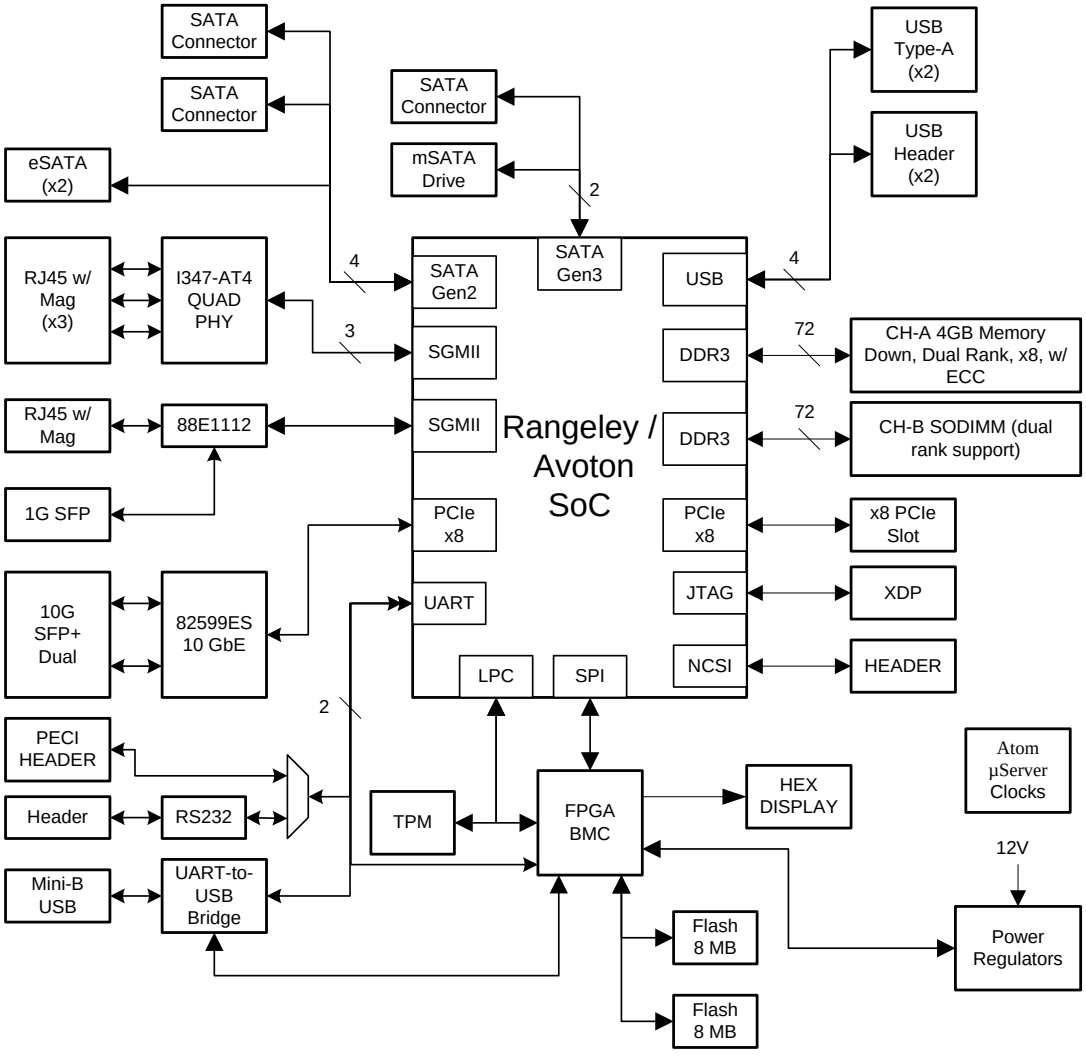

Figure 1 - RCC Block Diagram

1.2 Feature Summary

Feature	Description
Board Form Factor	12-layer Mini-ITX (6.7" X 6.7")
Processor	Supports all SKU's of Rangeley and Avoton CPU
Memory	• Dual Channel • Channel A – Memory Down, 4GB, DDR3L-1600, Dual Rank, with ECC • Channel B – SODIMM with ECC (1DPC Dual Rank)
Clocking	• IDT 9VRS4420 for Atom-based microservers • IDT 9ZXL0651 for PCIe clock distribution
Hard Drive	• Local mSATA Gen3 port • Two eSATA Gen2 ports • One internal SATA Gen3 port • Two internal SATA Gen2 ports
BIOS	• Redundant SPI Boot Flash • 16MB for main device • 8MB for failsafe device
USB	• Two back panel USB 2.0 ports • Two front panel USB 2.0 ports (through cable)
SOC UART	• One console port to CPU through a mini USB to UART bridge (Silicon Labs CP2105) • Optional RS232 UART through motherboard header

LAN support	• Four 10/100/1000Base-TX Ethernet Ports
	  ○ Three per Intel I347-AT4 quad PHY Controller
	  ○ One per Marvell 88E1112 PHY
	• Two 1G/10G SFP+ Ports per Intel 82599ES controller
	• One 100/1G SFP per Marvell 88E1112 PHY

Debug Interface	• XDP 60-pin debug interface
Expansion Ports	• One PCIe x8 Gen2 Slot • TPM Header
Battery	• Coin cell battery (CR2032) for RTC

On Board Management	• SmartFusion FPGA
	  ○ Power Sequencing
	  ○ Accessible through 2nd UART on CP2105
	  ○ Board Option Setting (Redundant SPI, 10G Power, etc…)

	○ Monitor Critical Signals ○ PORT80 Display ○ Fan Management (Future feature) ○ BMC/IPMI Support (Future feature)
Enclosure	• 8.9" X 3.5" X 8.3" Steel Enclosure with Aluminum bezel • Power and Reset Buttons • Power and HDD LED's • Support for one PCIe Card • Support for two 2.5" HDD • One 80mm fan
Power Supply	• Flex ATX Power Supply (Internal to Enclosure) • 220W Max • 100 - 240 VAC • 50 - 60Hz • 5-3 Amp
Temperature	• Temperature is 20°C to 35°C ambient outside enclosure[1]

[1] *RCC system operating range for the Alpha silicon stepping, should be within 20°C to 35°C during normal operation. The operating temperature for future stepping's is predicted to increase to meet NEBS level 3 qualification*

1.3 Enclosure Reference

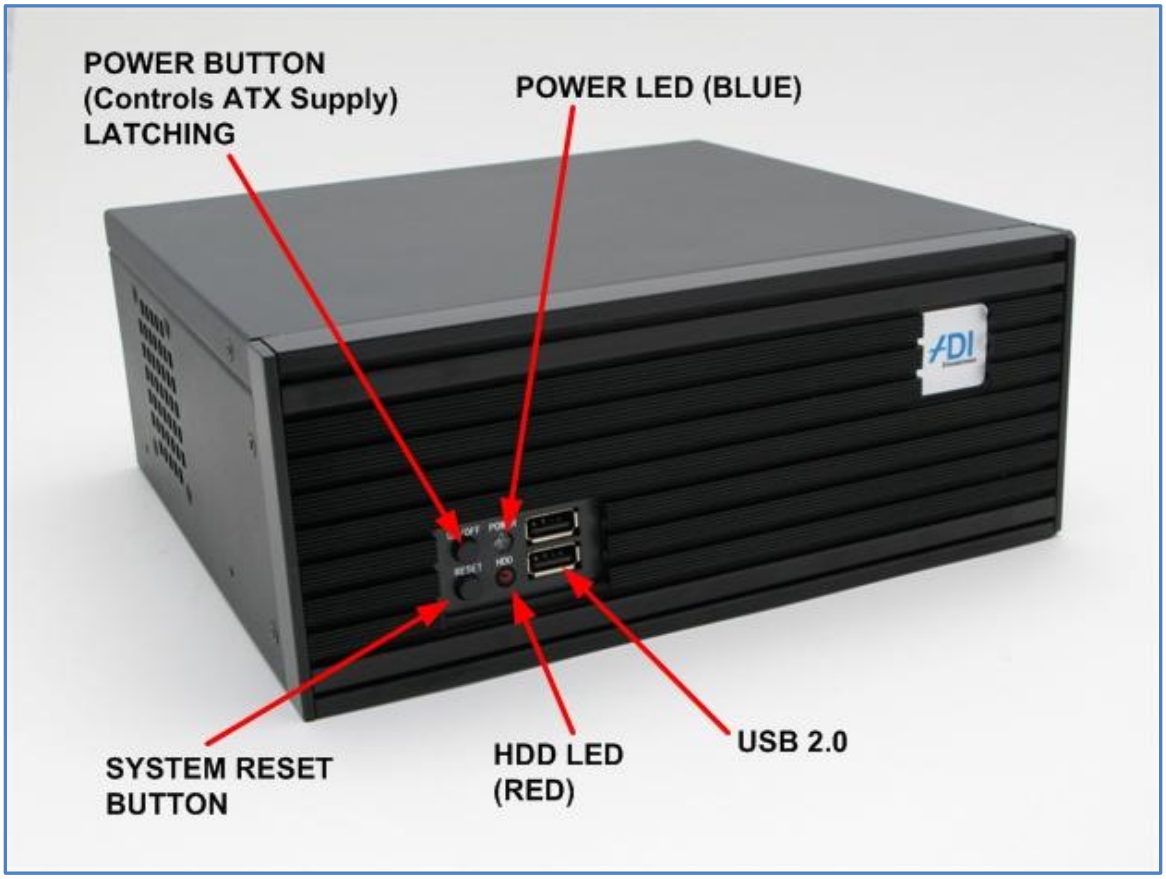

Figure 2 - Enclosure Front Panel

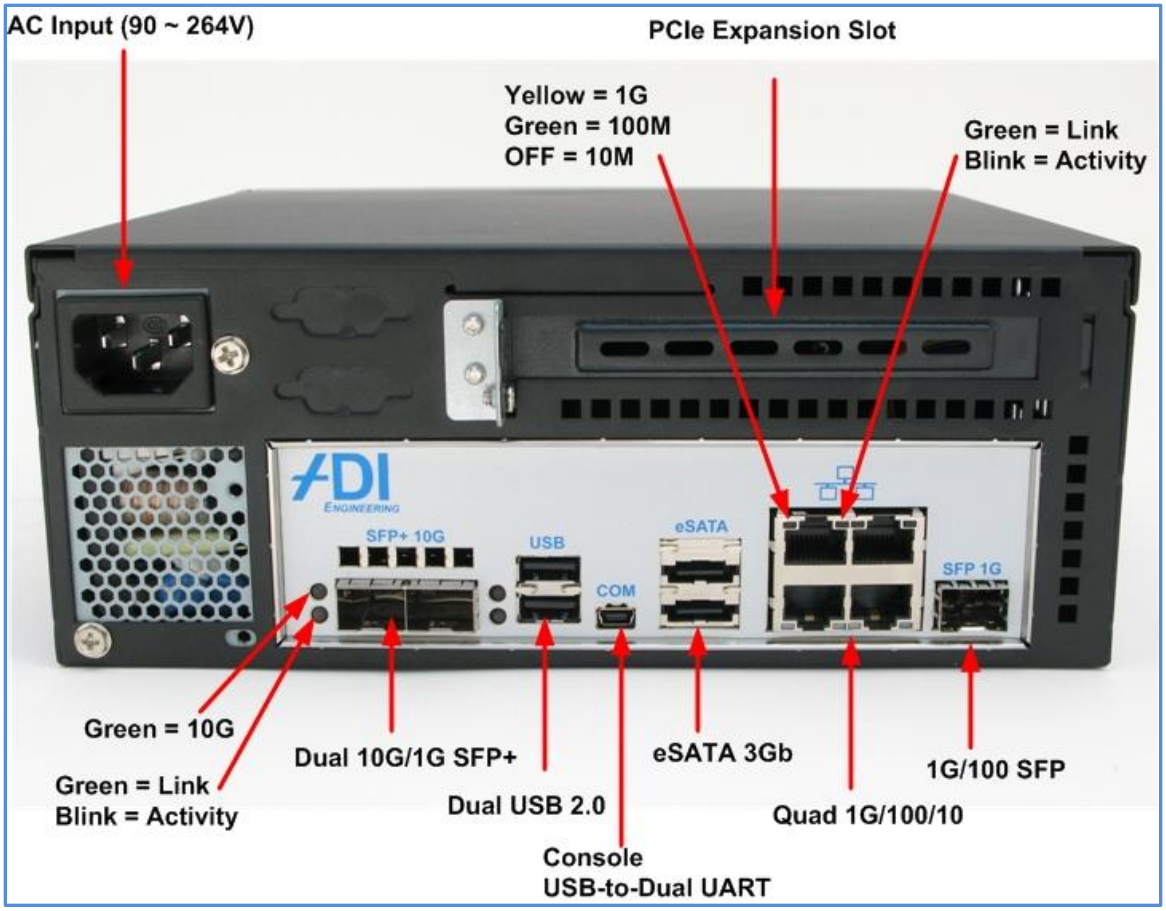

Figure 3 - Enclosure Back Panel

Figure 4 - Inside Enclosure

Figure 5 – Enclosure Cover, HDD Mount (HDD not provided with kit)

1.4 Component Layout Reference

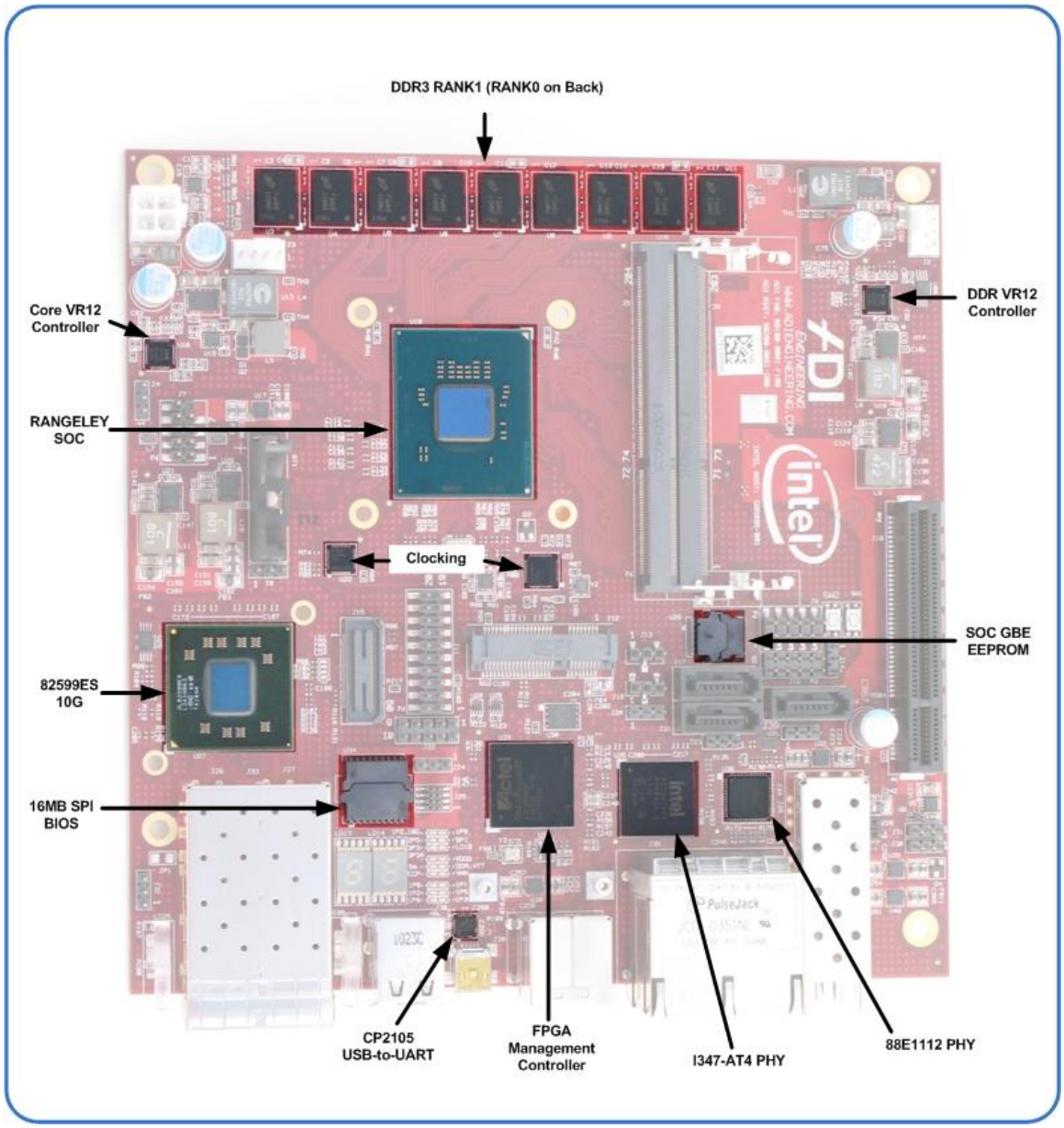

Figure 6 – Component Layout, Major ICs

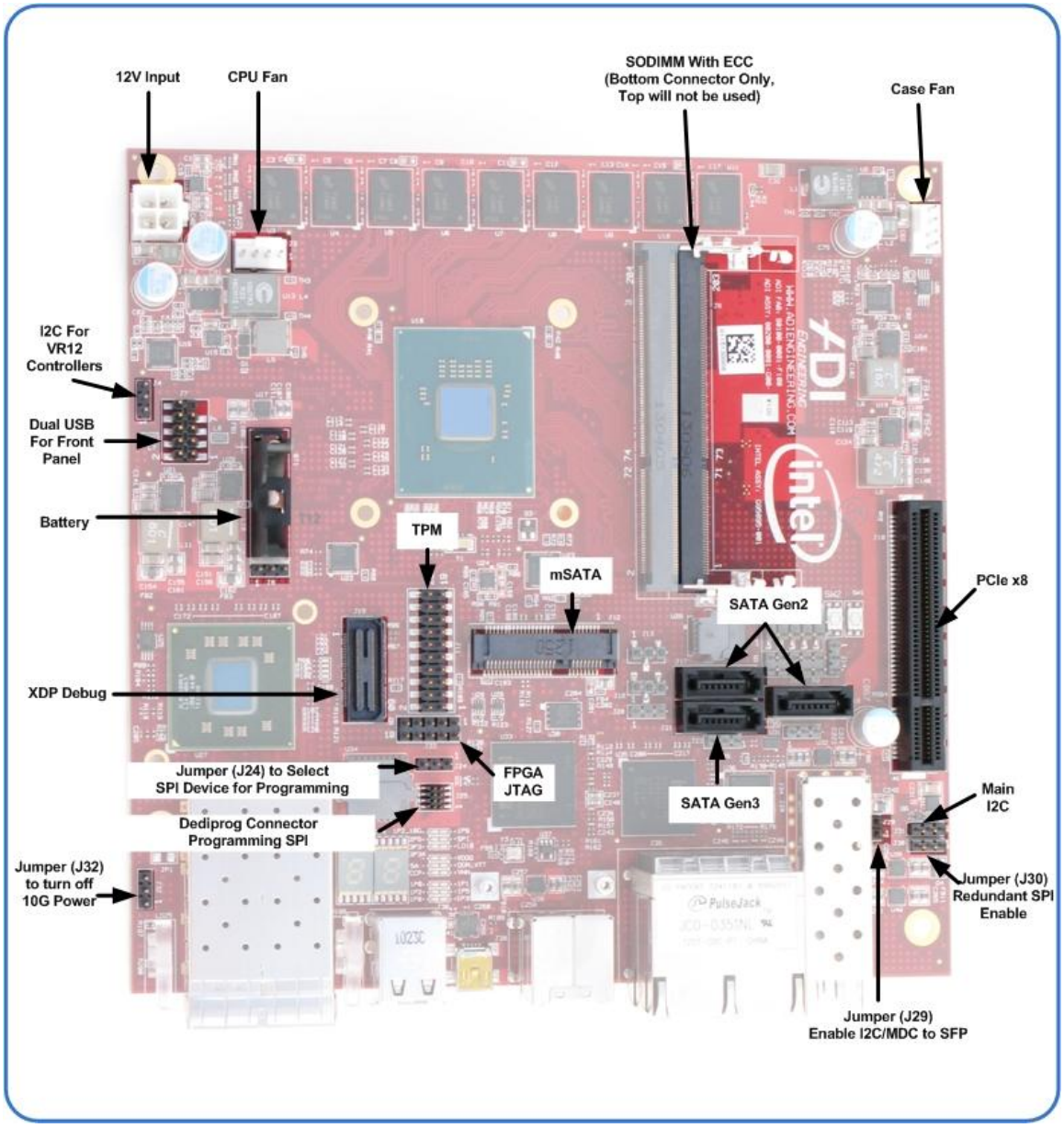

Figure 7 - Component Layout, Internal Connectors

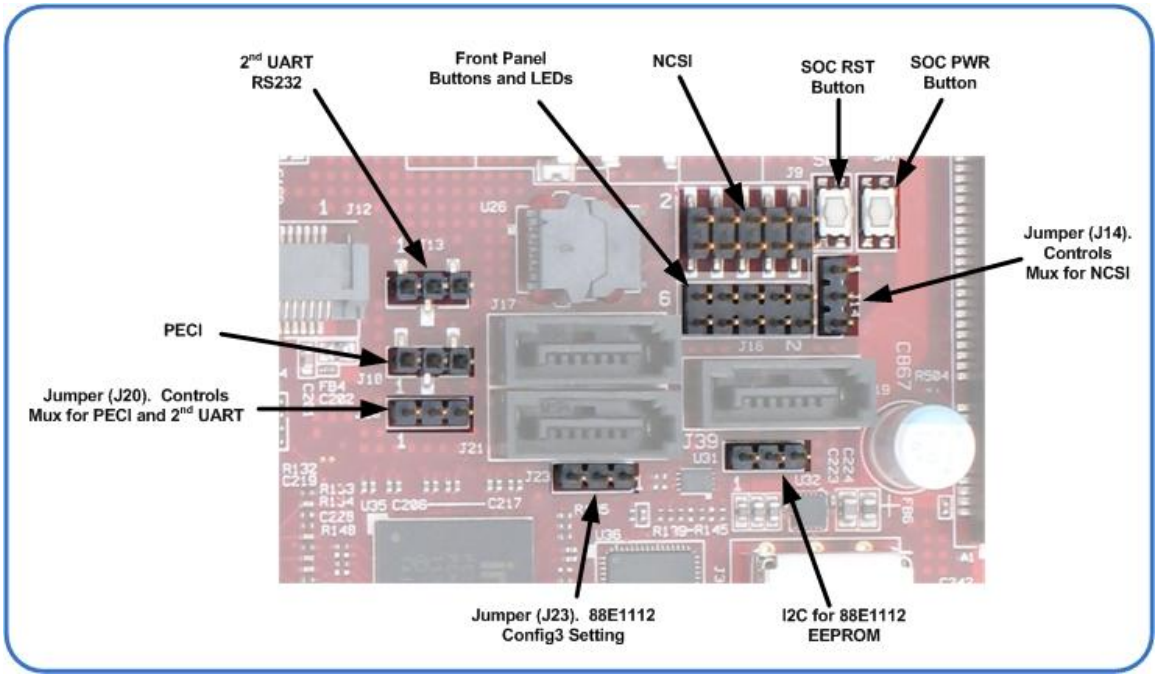
2nd UART RS232
Front Panel Buttons and LEDs
NCSI
SOC RST Button
SOC PWR Button
Jumper (J14). Controls Mux for NCSI
PECI
Jumper (J20). Controls Mux for PECI and 2nd UART
Jumper (J23). 88E1112 Config3 Setting
I2C for 88E1112 EEPROM

Figure 8 - Component Layout, Internal Connectors (cont)

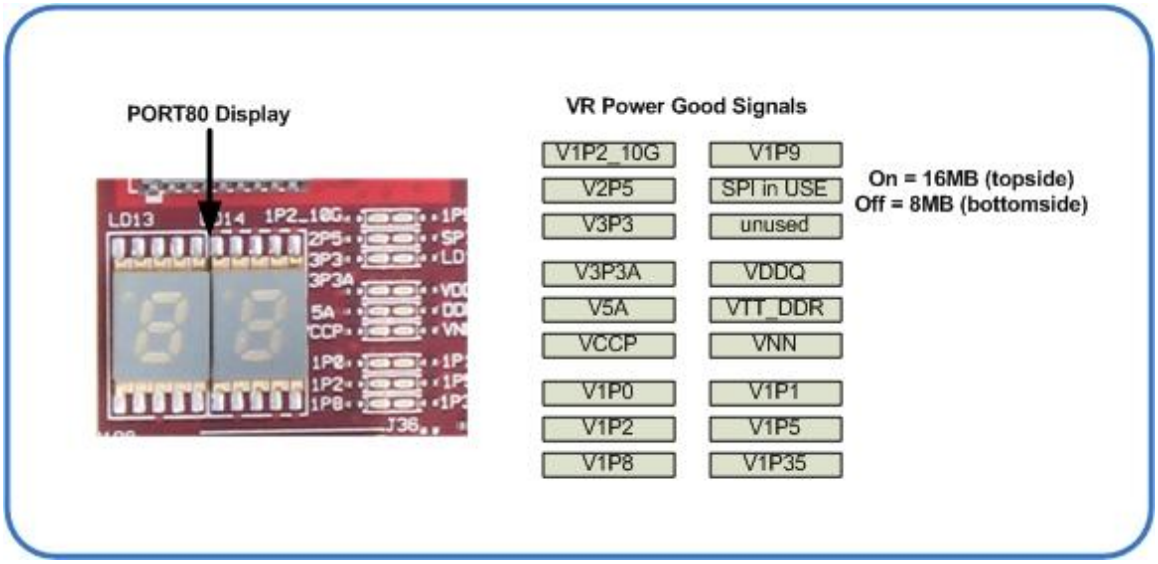

Figure 9 - Component Layout, Port80 and Debug LEDs

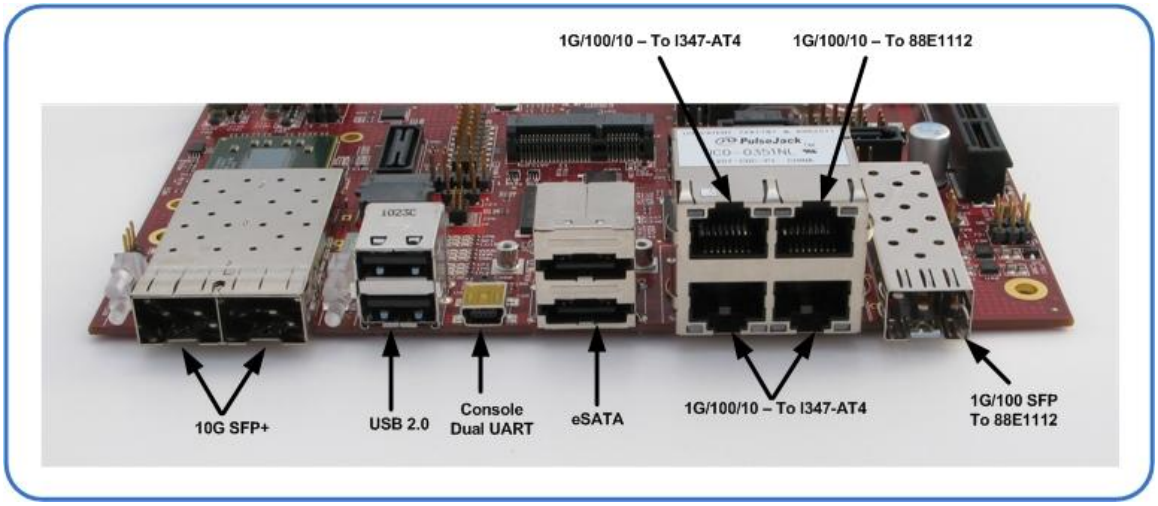

Figure 10 - Front Panel Connectors

1.5 Component Overview

1.5.1 Rangeley SOC

The RCC system ships with the highest core count SKU of the Rangeley SoC. Please refer to the latest Intel documentation on the SoC for the SKU features. The RCC system has been designed to be compatible with all other Rangeley SKUs as well, inclusive of lower core count SKUs.

1.5.2 Memory

The RCC supports two channels of DDR3. These channels are configured as follows:

- Channel-A – Is memory down (soldered to board), configured as 4GB, Dual Rank, 1600MT/s, ECC, 1.35V (18 total devices)
- Channel-B – Is a SODIMM. Supported SODIMM is a 4GB, Dual Rank, 1600MT/s, ECC, 1.35V

A requirement of the SOC is that channel-B must be equal to channel-A for density, rank, speed, ECC, and type (i.e. UDIMM, SODIMM, etc..). The BIOS gets this information by reading and comparing the SPD EEPROMs for each channel. A SPD EEPROM was placed on the board for channel-A. Channel-A was routed as a UDIMM to simplify the layout so the starting SPD was based on Micron MT18KSF51272AZ-1G6. That SPD was then modified to change the type (byte 0x3 in SPD EEPROM) from a UDIMM (0x2) to a 72b-SO-UDIMM (0x8). The CRC for the SPD was then recalculated.

The RCC system ships with 8GB of memory. The board could support up to 16GB of memory by changing the memory down devices, SPD, and SODIMM.

1.5.3 82599ES (Dual 10G Controller)

The 10Gb Ethernet controller is connected to the SOC with a PCIe x8 Gen2 interface. It provides access to two SFP+ slots. There is a configuration EEPROM (32KB) which configures the device for SFI with no management. There is also an optional flash device (currently no used), that could hold an option ROM for PXE boot.

This device and its surrounding circuits can be completely powered down, by setting a jumper on the board or configuring the board management setting over the management console.

1.5.4 I347-AT4 (Quad GBE PHY)

The SOC is connected to the Intel I347-AT4 quad PHY over SGMII. It configures the PHY using a MDC/MDIO interface. Three of the SOC MAC interfaces are connected to this PHY:

- SGMII-0
- SGMII-2
- SGMII-3

The PHY is then connected to an RJ45 with integrated magnetics.

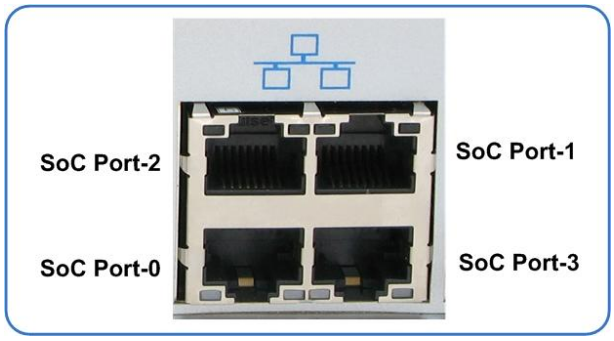

Figure 11 - SoC Ethernet port mapping

1.5.5 88E1112 (Single GBE PHY)

The SOC is connected to the Marvell 88E1112 over SGMII-1. It configures the PHY using a MDC/MDIO interface. This PHY is connected to an RJ45 with integrated magnetics and to an SFP slot. It supports Auto Media Detection between the two interfaces[2].

1.5.6 CP2105 (Dual USB-to-UART Bridge)

The RCC board has a CP2105 which is a dual USB-to-UART bridge. One UART is connected to the console port on the SOC and the second UART is connected to the management FPGA.

[2] SW Driver is still under development to support Auto Media Detection feature

1.5.7 SOC EEPROM

The SOC uses an EEPROM to configure the Ethernet MAC interfaces. Please refer to Intel representative for the latest EEPROM image for the RCC board.

1.5.8 SOC SPI Flash Devices

There are two SPI Flash devices connected to the SOC. There is 16MB device which is used for the main SPI flash image. It contains a BIOS and descriptor which is used for normal operation and can be updated with new versions. There is an 8MB device that is used as a failsafe SPI flash image to provide redundant boot functionality. This device cannot be updated and is used only when the main device fails. The redundant boot function is controlled by the FPGA and can be enabled/disabled by a jumper or configuring the board management settings over the management console.

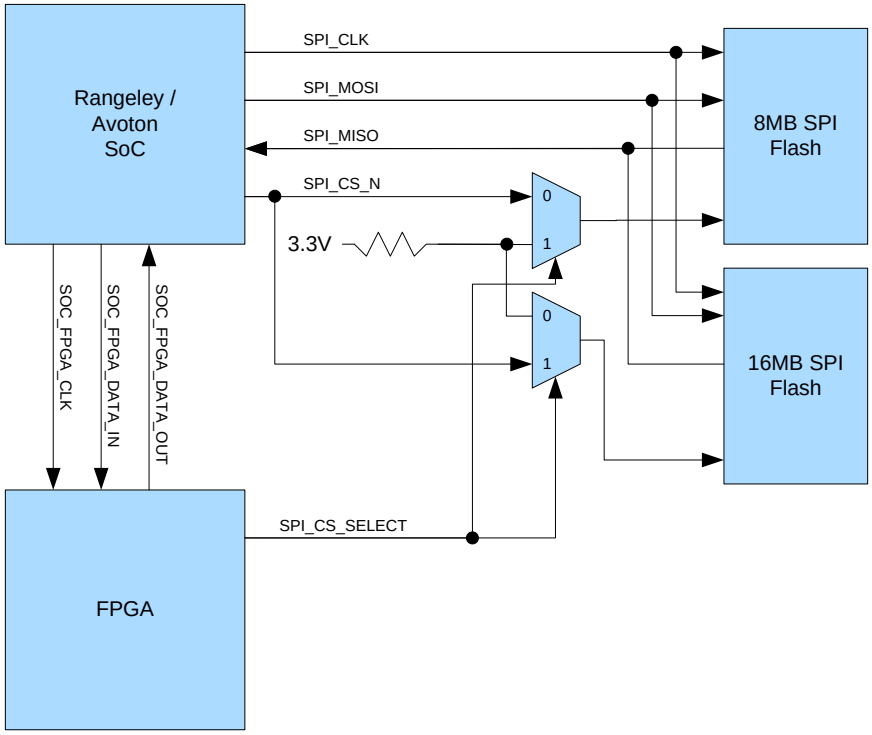

Figure 12 - Redundant SPI FLash

1.5.9 Management FPGA

The board management FPGA performs the following functions:

- Power Sequencing
- Redundant SPI
- Board Settings

- Analog Measurements (Temperature, Voltage, Current)
- Monitors Critical Signals
- Manufacturing Information

The FPGA can report status and the user can change settings using the UART connected to the USB-to-UART bridge. Refer to section 2.3 for operation details. The hardware could support the following features with a firmware upgrade:

- BMC/IPMI Support
- Serial Over LAN
- FAN Monitoring and Control
- Remote FPGA updates

1.5.10 PCIe Slot

The RCC board has a PCIe x8 expansion card. The chassis supports a full-height, half-length PCIe x16 card. The board is designed to support up to a 75W card[3]. A x8-to-x16 riser card is supplied with the kit to mount the card in the enclosure.

[3] Thermal testing has only been completed with a 15W card.

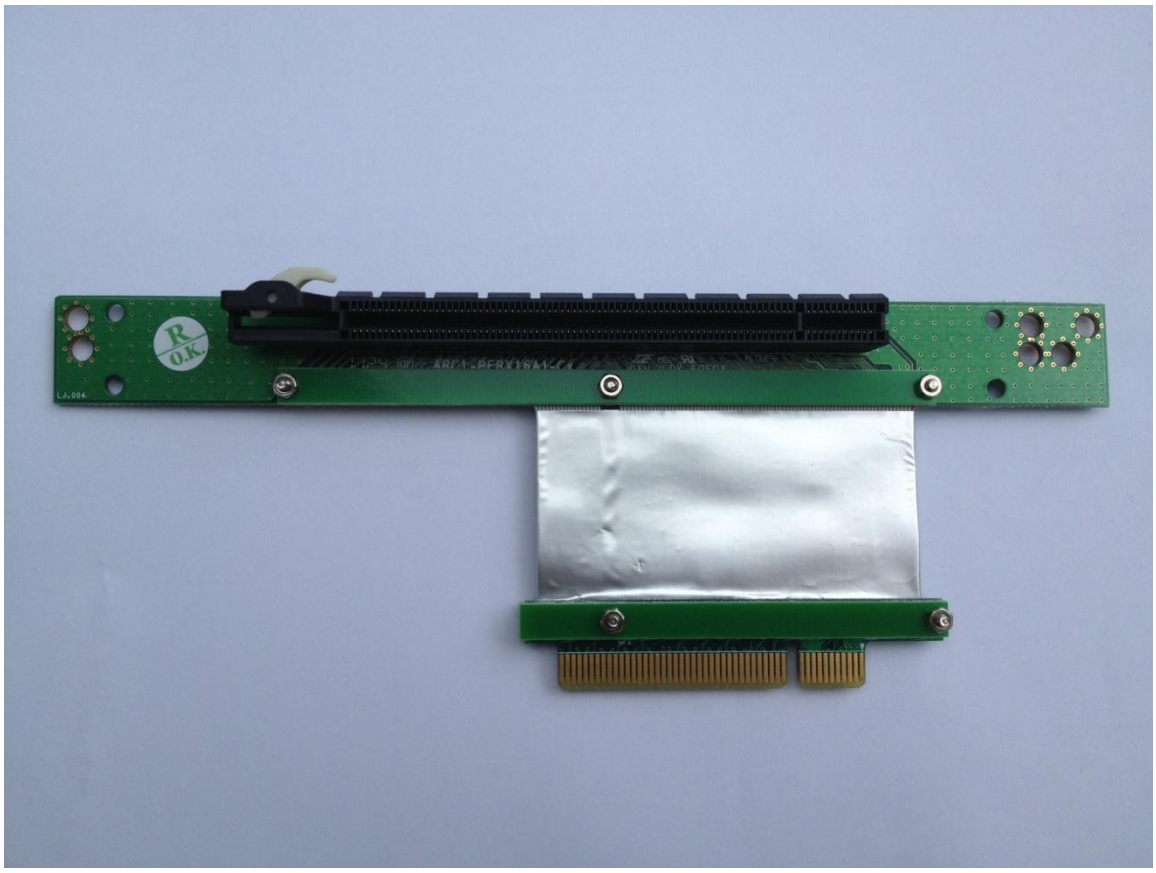

Figure 13 - PCIe x8 to x16 Riser Card

1.5.11 Battery

The RCC board contains a standard CR2032 coin cell battery to support the RTC.

1.5.12 TPM

The RCC board has 2x7 connector for a TPM module.

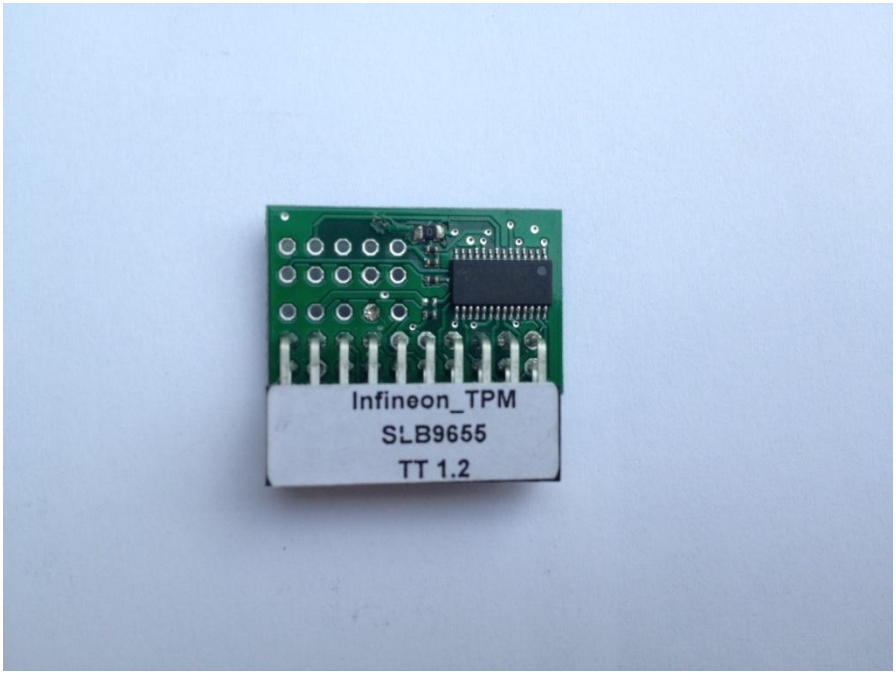

Figure 14 - TPM Module

1.6 Connector and Jumper Reference

1.6.1 Power Connector (J1)

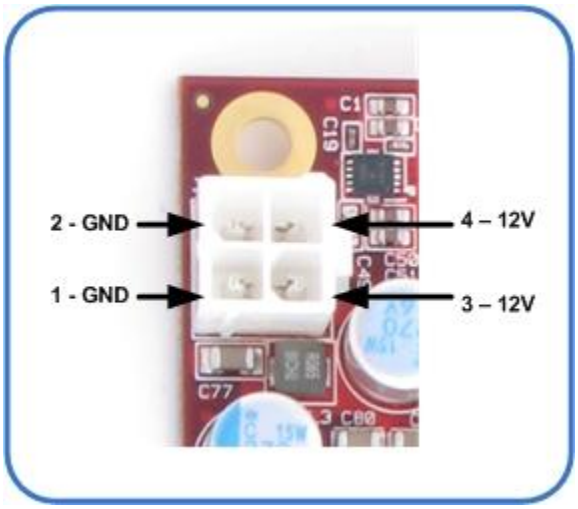

Figure 15 - Connector: Power (J1)

1.6.2 Fan Connecters (J3 & J2)

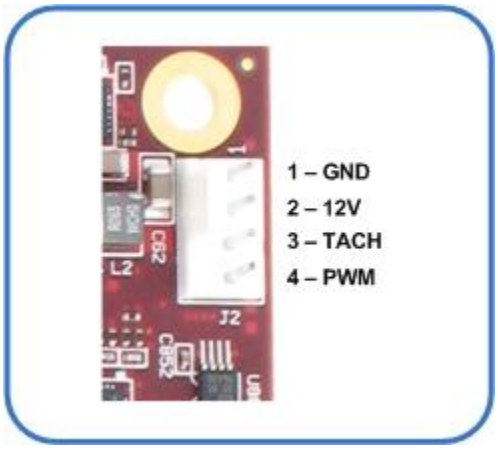

Figure 16 - Connector: Fan (J3 & J2)

1.6.3 USB Front Panel Connector (J7)

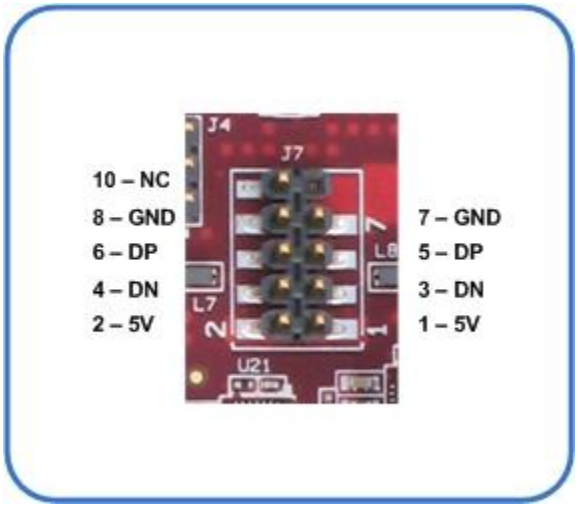

Figure 17 - Connector: USB Front Panel (J7)

1.6.4 VR12 I2C Connector (J4)

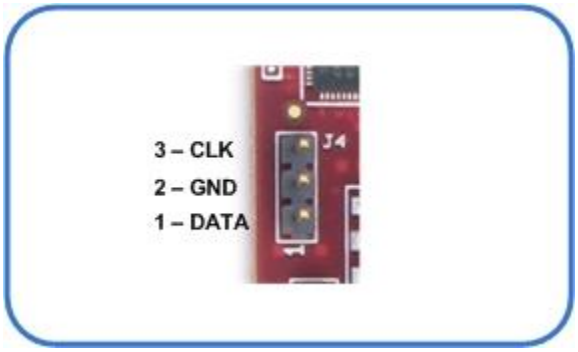

Figure 18 - Connector: VR12 I2C (J4)

1.6.5 Jumper – 10G Enable/Disable (J32)

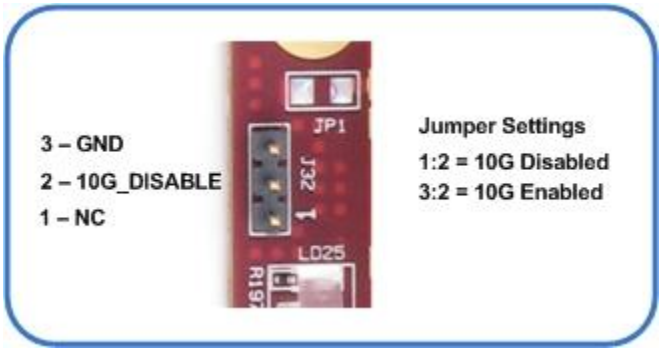

Figure 19 - Jumper: 10G Enable/Disable (J32)

1.6.6 TPM Connector (J11)

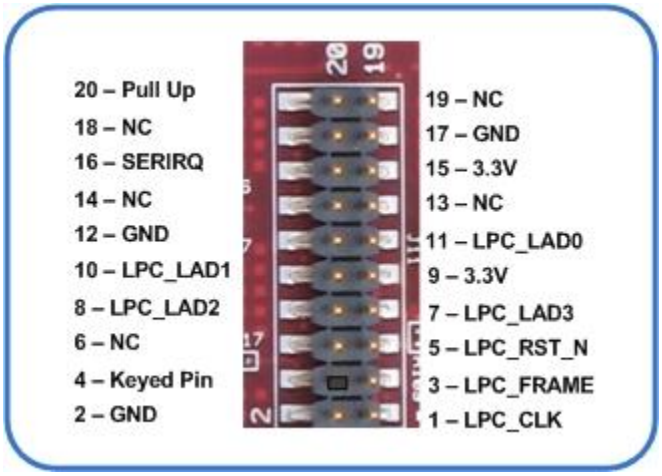

Figure 20 - Connector: TPM (J11)

1.6.7 In-Circuit SPI Connector (J25) and Jumper (J24)

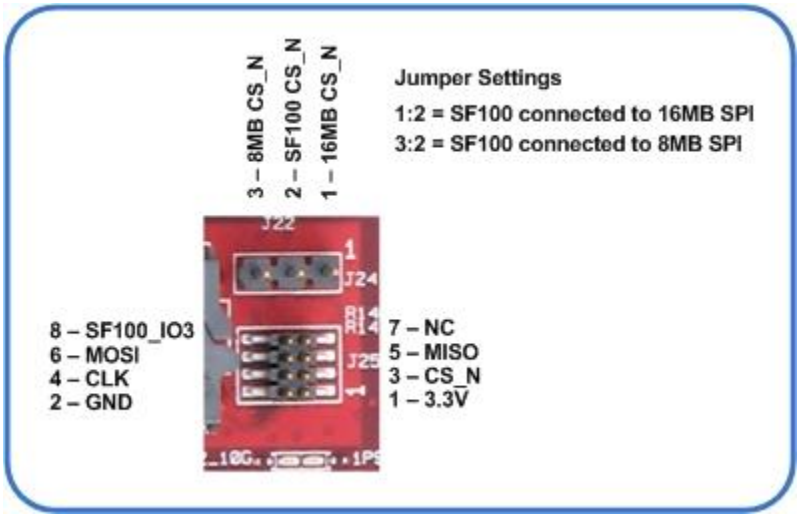

Figure 21 - Connector: SPI (J25), Jumper: SPI (J24)

1.6.8 FPGA JTAG Connector (J22)

Figure 22 - Connector: FPGA JTAG (J22)

1.6.9 RS232 UART Connector (J13), PECI Connector (J18), UART/PECI Jumper (J20)

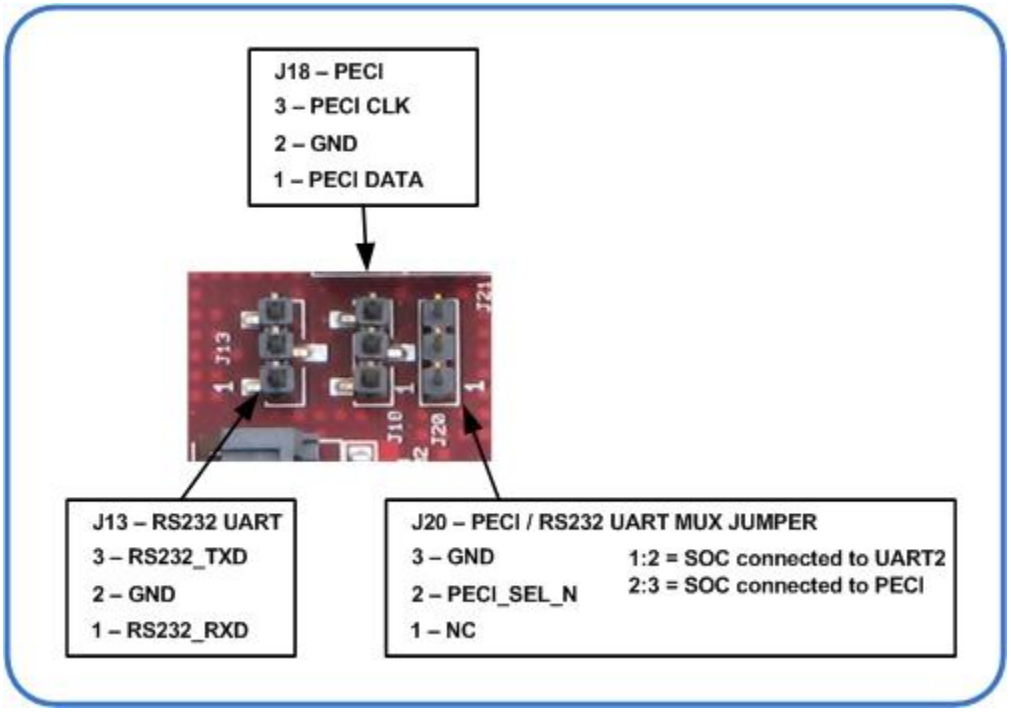
J18 – PECI
3 – PECI CLK
2 – GND
1 – PECI DATA
J13 – RS232 UART
3 – RS232_TXD
2 – GND
1 – RS232_RXD
J20 – PECI / RS232 UART MUX JUMPER
3 – GND
2 – PECI_SEL_N
1 – NC
1:2 = SOC connected to UART2
2:3 = SOC connected to PECI

Figure 23 - Connector: RS232 (J13), PECI (J18), Jumper PECI/RS232 (J20)

1.6.10 Jumper – 88E1112 CONFIG3 (J23)

Figure 24 - Jumper: 88E1112 TWSI Configuration (J23)

1.6.11 NCSI Connector (J9), Front Panel Connector (J16), NCSI Jumper (J14)

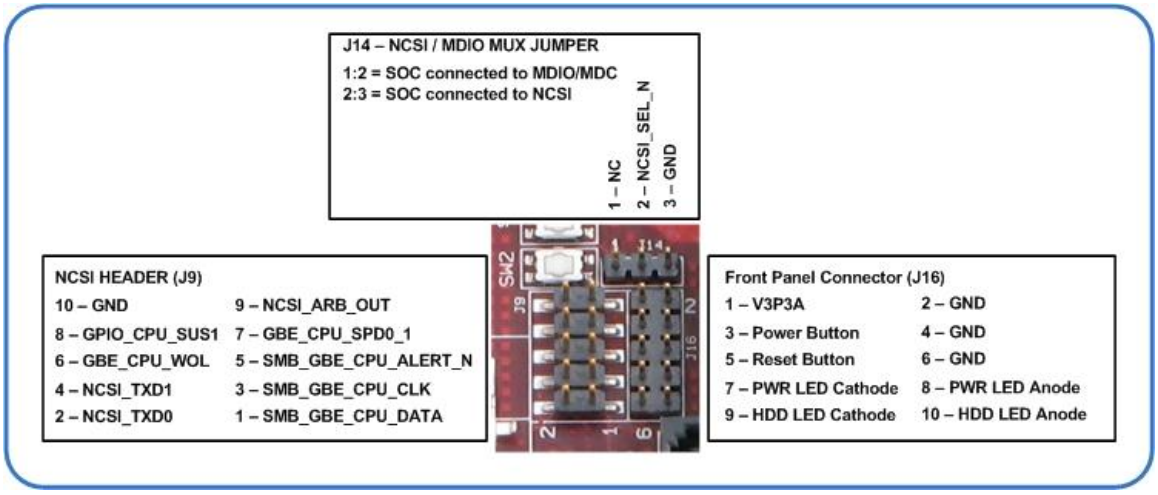

Figure 25 - Connector: NCSI Header (J9), Front Panel (J16), Jumper NCSI/MDIO (J14)

Schematic Signal	NCSI Function	NCSI Pin Direction	Notes
SMB_GBE_CPU_DATA	NCSI_TX_EN	I	
SMB_GBE_CPU_CLK	NCSI_CLK_IN	I	
SMB_GBE_CPU_ALERT_N	NCSI_CRS_DV	O	
GBE_CPU_SDP0_1	NCSI_ARB_IN	I	
NCSI_TXD0	NCSI_TXD0	I	
NCSI_TXD1	NCSI_TXD1	I	
GPIO_CPU_SUS1	NCSI_RXD0	O	
GBE_CPU_WOL	NCSI_RXD1	O	
NCSI_ARB_OUT	NCSI_ARB_OUT	O	

Table 1 - NCSI Connector

1.6.12 SMBus Connector (J31), Redundant Boot Jumper (J30)

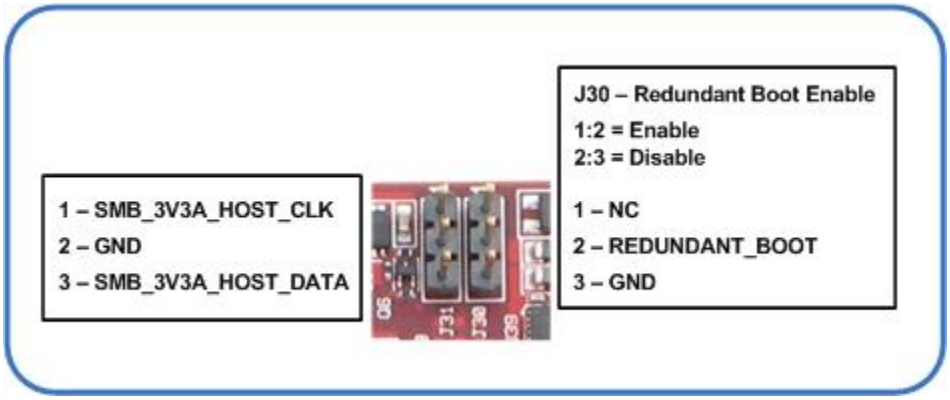

Table 2 - Connector: Main SMB (J31), Jumper: Redundant Boot (J30)

2 RCC SETUP AND USE

2.1 Serial Port Drivers

The RCC has a USB-to-UART bridge for the CPU console and FPGA management console. The device used is a Silicon Labs CP2105. Before connecting the RCC system, the host computer will need to install drivers for the CP2105. Follow these instructions:

1. Go to the following address:
   http://www.silabs.com/products/interface/usbtouart/Pages/usb-to-uart-bridge.aspx
2. Select **Tools** tab.
3. Select drivers for your OS. For Windows, select **CP210x_VCP_Windows.zip**
4. Download and following instructions for installing driver
5. Use the provided USB Mini-B cable and connect the RCC system console to the host computer
6. Verify that host computer can see two additional serial ports
7. The first serial port added to the host computer will connect to the FPGA management console. The second serial port will connect to the CPU console.

The user will need to use a terminal emulator (i.e. Hyperterminal, PuTTy) to connect to the consoles. The settings for the terminal should be the following:

- Speed = 115,200
- Data Bits = 8
- Parity = None
- Stop Bits = 1
- Flow Control = None
- Preferred emulation mode is ANSI

2.2 Running Yocto Linux

The RCC system comes with a mSATA drive with a custom Yocto Linux installation and is ready to use out of the box. For instructions on how to create Yocto Linux with Rangeley patches and drivers, please refer to Intel documentation.

1. Connect User Interface. Two options:
   a. CPU console port over USB-to-UART bridge
   b. Graphics Card in PCIe slot, USB Keyboard
2. Connect AC power cable
3. Press power button on front panel.
4. If using the CPU console port, debug messages should be displayed as the BIOS boots. IF using a graphics card, nothing will be displayed until the BIOS splash screen.
5. Press **ESC** when requested by the BIOS to enter the BIOS setup screen

6. Go to **Boot** menu and verify that **Boot Option #1** is set to boot mSATA (i.e. **UEFI: M4-CT032M4SSD3**). If not, change boot option #1 to mSATA.
7. Go to **Save & Exit** and select **Save Changes and Exit**
8. System should boot Yocto Linux. Type **root** when at command prompt. There is no password.

2.3 Management Console

The RCC board has a management console which is connected to the on-board FPGA over the USB-to-UART bridge. The initial version of this management console provides board status information to the user. This console is still under development and will provide the following features in the future:

- User configurable settings for on-board jumpers (i.e. Redundant SPI, 10G Power, etc..)
- FPGA update over UART
- Additional board status (i.e. Information from Rangeley PECI, Manufacturing Information)

More advanced features that are under consideration

- BMC/IPMI Support
- Serial OverLAN
- FAN Monitoring and Control

Instructions to access management console:

1. Follow instructions in section 2.1 for connecting to serial port. Management console is the first UART.
2. Power on RCC system
3. You should see management console displayed

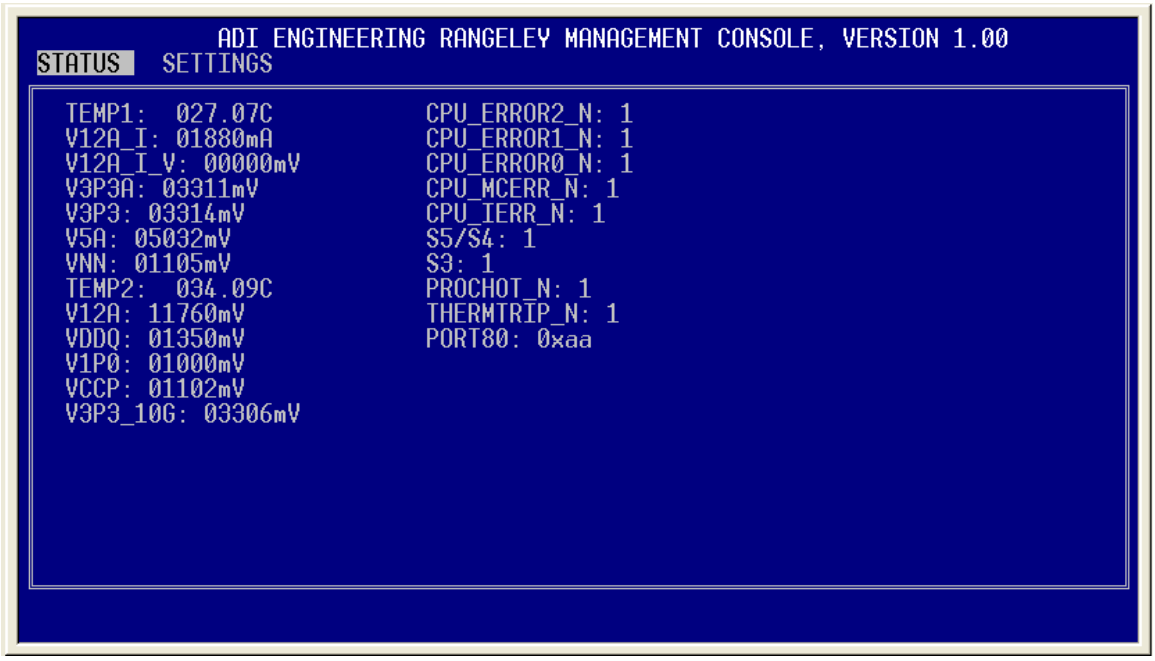

Figure 26 - FPGA Management Console

4. You can navigate console with arrow keys and select or toggle an item with the ENTER key.

2.4 Updating BIOS

2.4.1 Updating Flash with a SPI Programmer

Both the 16MB and 8MB SPI flash devices can be updated using an external programmer. The tools required to update the flash devices are below:

- Dediprog SF100 (http://www.dediprog.com/SPI-flash-in-circuit-programming/SF100)
- 1.27mm Cable Adapter (http://www.dediprog.com/SPI-flash-in-circuit-programming/ISP-Cable-Adaptor)
- Host computer with Windows OS and Dediprog software installed. Dediprog software is located at (http://www.dediprog.com/SPI-flash-in-circuit-programming/SF100) under **Software Download** tab.
- SPI Flash binary with descriptor and BIOS. Available from Intel and ADI

Figure 27 - DediProg SF100 with 1.27mm Adapter

Instructions for updating SPI Flash

1. Turn off power to RCC system. No external power is required for updating SPI flash
2. Remove enclosure cover. Held on by two screws.
3. Set the jumper (J24) to the SPI flash you want accessible to the external programmer. This example starts with the 8MB device.

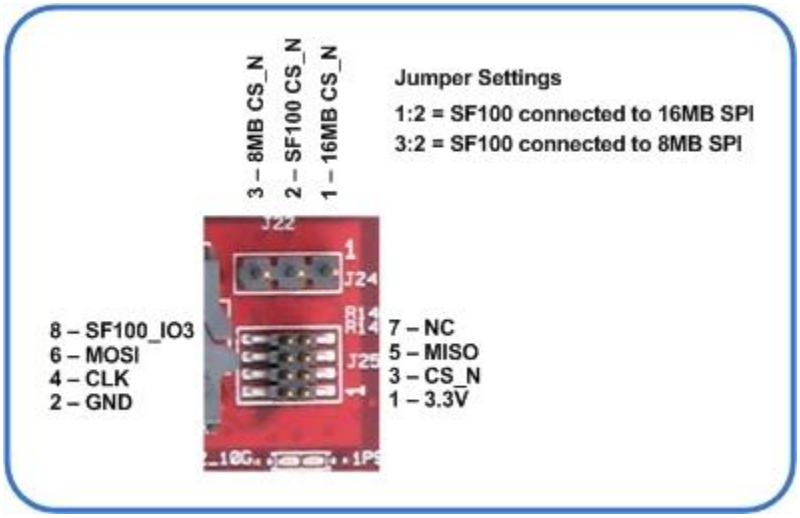

Figure 28 - Jumper for SPI Flash programming

4. Connect Dediprog to the RCC board. Pay attention that pin-1 on the board lines up with the red-wire on the adapter cable.

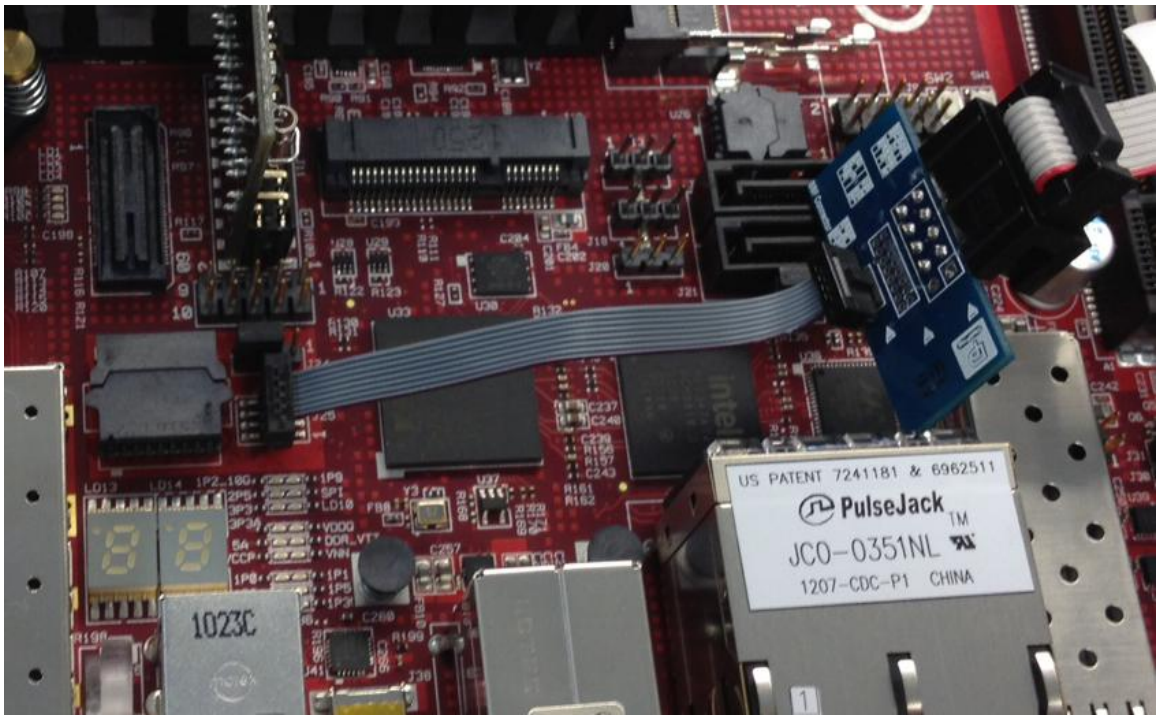

Figure 29 - DediProg connected to board

5. Start **DediProg Engineering** software:

6. The software should auto detect the flash. Select **W25Q64CV** for the 8MB device.

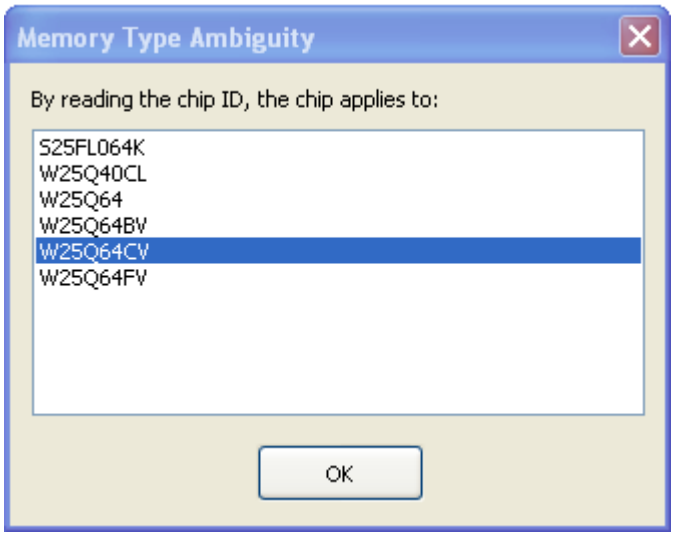

Figure 30 - DediProg Flash Detection, 8MB

7. Select **File** icon in the tool bar and select the binary file to be programmed into the flash. Select **Raw Binary**. Select **OK**.

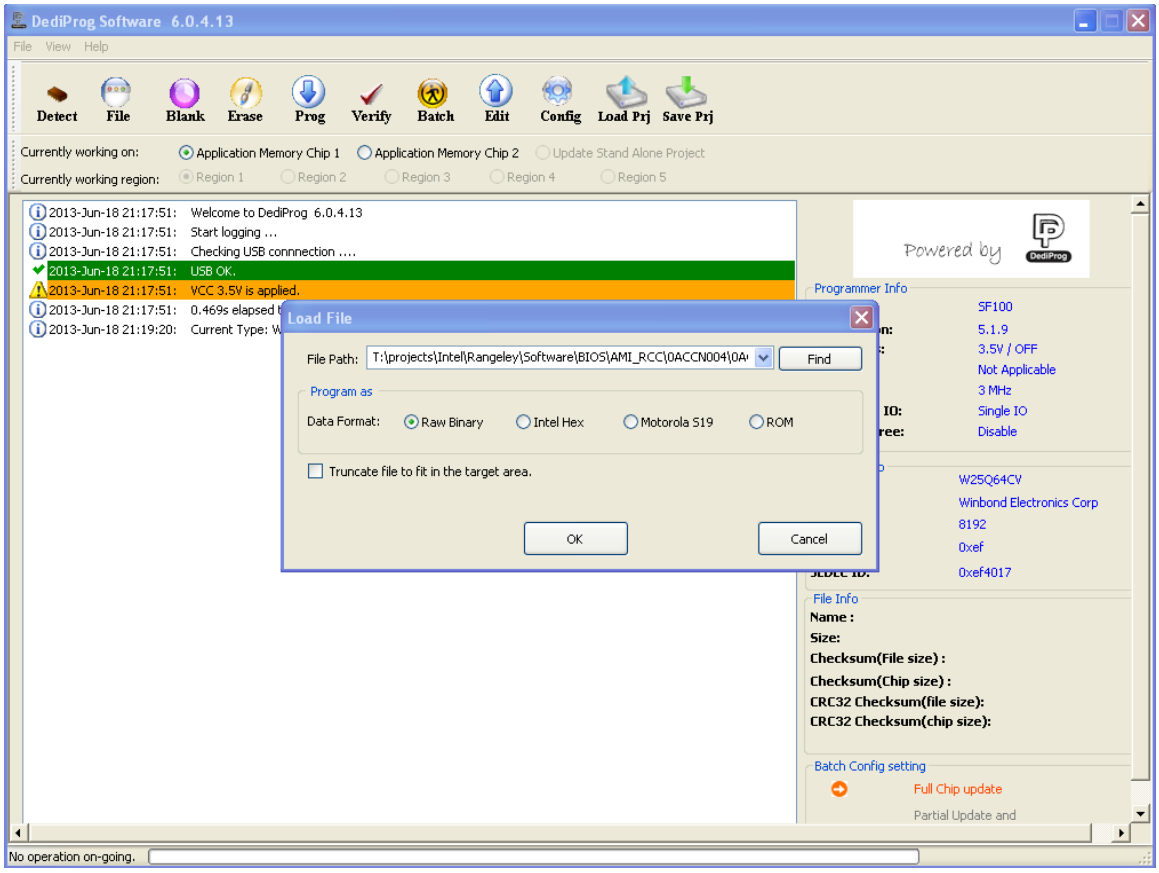

Figure 31 - Loading Dediprog SPI File

8. Select **Erase** icon in the tool bar to erase flash contents

Figure 32 - DediProg Erase Flash

9. Select **Prog** icon in the tool bar to write file to flash

Figure 33 - DediProg Program Flash

10. Select **Verify** icon in the tool bar to compare flash contents with binary file. Verify that tool reports **Checksum Identical**.

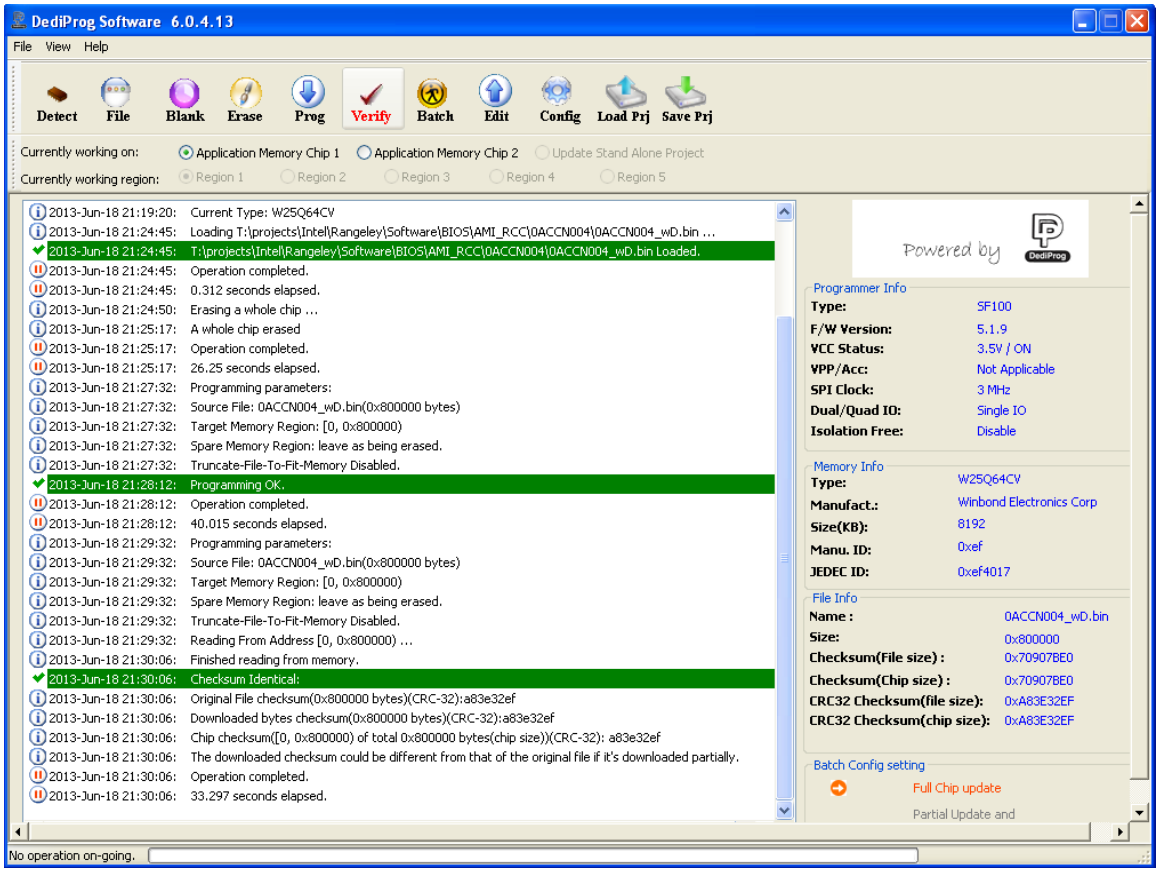
DediProg Software 6.0.4.13
File View Help
Detect File Blank Erase Prog Verify Batch Edit Config Load Prj Save Prj
Currently working on: Application Memory Chip 1 Application Memory Chip 2 Update Stand Alone Project
Currently working region: Region 1 Region 2 Region 3 Region 4 Region 5
2013-Jun-18 21:19:20: Current Type: W25Q64CV
2013-Jun-18 21:24:45: Loading T:\projects\Intel\Rangeley\Software\BIOS\AMI_RCC\0ACCN004\0ACCN004_wD.bin ...
2013-Jun-18 21:24:45: T:\projects\Intel\Rangeley\Software\BIOS\AMI_RCC\0ACCN004\0ACCN004_wD.bin Loaded.
2013-Jun-18 21:24:45: Operation completed.
2013-Jun-18 21:24:45: 0.312 seconds elapsed.
2013-Jun-18 21:24:50: Erasing a whole chip ...
2013-Jun-18 21:25:17: A whole chip erased
2013-Jun-18 21:25:17: Operation completed.
2013-Jun-18 21:25:17: 26.25 seconds elapsed.
2013-Jun-18 21:27:32: Programming parameters:
2013-Jun-18 21:27:32: Source File: 0ACCN004_wD.bin(0x800000 bytes)
2013-Jun-18 21:27:32: Target Memory Region: [0, 0x800000)
2013-Jun-18 21:27:32: Spare Memory Region: leave as being erased.
2013-Jun-18 21:27:32: Truncate-File-To-Fit-Memory Disabled.
2013-Jun-18 21:28:12: Programming OK.
2013-Jun-18 21:28:12: Operation completed.
2013-Jun-18 21:28:12: 40.015 seconds elapsed.
2013-Jun-18 21:29:32: Programming parameters:
2013-Jun-18 21:29:32: Source File: 0ACCN004_wD.bin(0x800000 bytes)
2013-Jun-18 21:29:32: Target Memory Region: [0, 0x800000)
2013-Jun-18 21:29:32: Spare Memory Region: leave as being erased.
2013-Jun-18 21:29:32: Truncate-File-To-Fit-Memory Disabled.
2013-Jun-18 21:29:32: Reading From Address [0, 0x800000) ...
2013-Jun-18 21:30:06: Finished reading from memory.
2013-Jun-18 21:30:06: Checksum Identical:
2013-Jun-18 21:30:06: Original File checksum(0x800000 bytes)(CRC-32):a83e32ef
2013-Jun-18 21:30:06: Downloaded bytes checksum(0x800000 bytes)(CRC-32):a83e32ef
2013-Jun-18 21:30:06: Chip checksum([0, 0x800000) of total 0x800000 bytes(chip size))(CRC-32): a83e32ef
2013-Jun-18 21:30:06: The downloaded checksum could be different from that of the original file if it's downloaded partially.
2013-Jun-18 21:30:06: Operation completed.
2013-Jun-18 21:30:06: 33.297 seconds elapsed.
Powered by DediProg
Programmer Info
Type: SF100
F/W Version: 5.1.9
VCC Status: 3.5V / ON
VPP/Acc: Not Applicable
SPI Clock: 3 MHz
Dual/Quad IO: Single IO
Isolation Free: Disable
Memory Info
Type: W25Q64CV
Manufact.: Winbond Electronics Corp
Size(KB): 8192
Manu. ID: 0xef
JEDEC ID: 0xef4017
File Info
Name : 0ACCN004_wD.bin
Size: 0x800000
Checksum(File size) : 0x70907BE0
Checksum(Chip size) : 0x70907BE0
CRC32 Checksum(file size): 0xA83E32EF
CRC32 Checksum(chip size): 0xA83E32EF
Batch Config setting
Full Chip update
Partial Update and
No operation on-going.

Figure 34 - DediProg Verify

11. If updating the 16MB device, set jumper (J24) to 16MB and repeat steps. The device selected should be **N25Q128A13**.
12. Disconnect DediProg from RCC board.

2.4.2 Updating BIOS from EFI Shell

1. Download AMI BIOS update utility
    a. Go to http://ami.com/support/
    b. Select **Technical Support**
    c. Under **AMIBIOS**, select **Aptio**, then **SUBMIT**
    d. Select **AMIBIOS & Aptio – AMI Firmware Update Utility** and follow instructions to download utility.
2. Place this utility on a USB flash drive along with the BIOS binary. (**NOTE: BIOS binary will be smaller than the 8MB or 16MB images and does not have descriptor**).
3. Insert USB flash drive into RCC system.
4. Power on RCC system
5. Press **ESC** when requested by the BIOS to enter the BIOS setup screen
6. Go to **Save & Exit** and under **Boot Override** select **UEFI: Built-in EFI Shell**

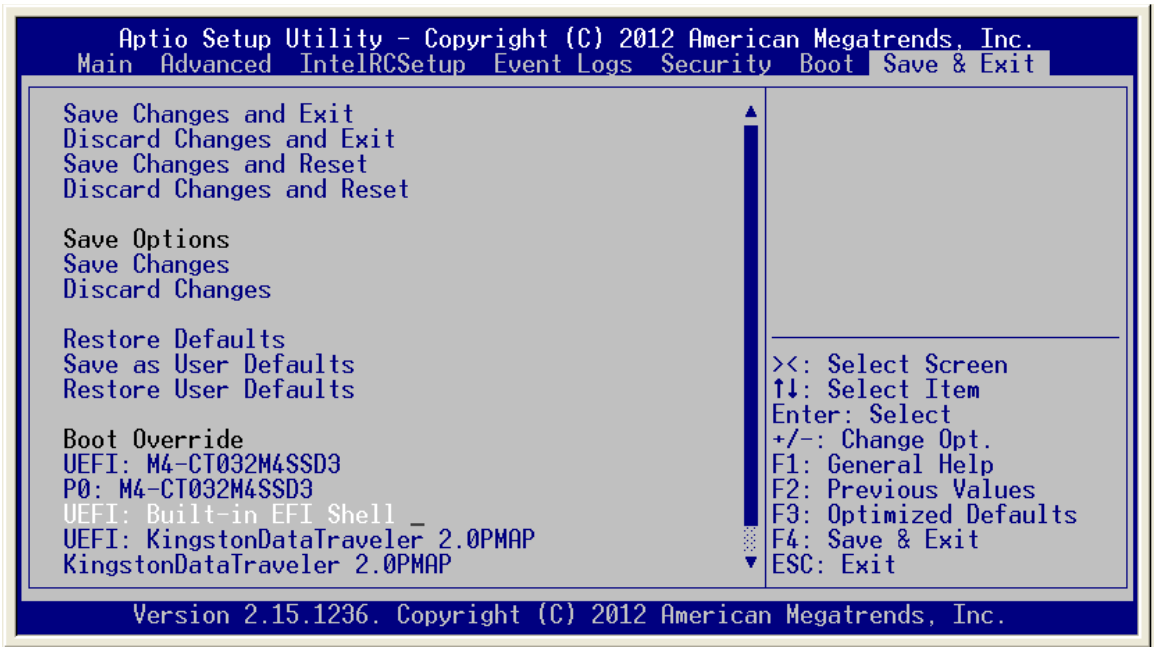

Figure 35 - BIOS, boot Built-in EFI Shell

7. USB flash drive will be identified as a **fs** device and labeled as a **Removable HardDisk**. In this example, the USB flash drive is fs1.

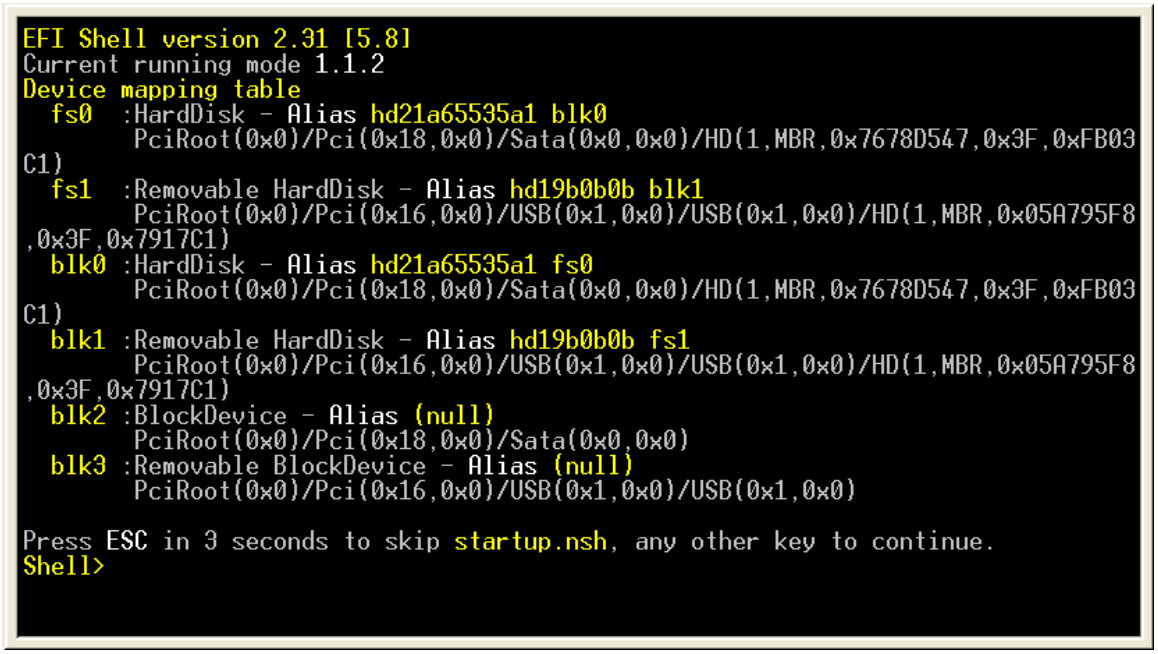
EFI Shell version 2.31 [5.8]
Current running mode 1.1.2
Device mapping table
fs0 :HardDisk - Alias hd21a65535a1 blk0
PciRoot(0x0)/Pci(0x18,0x0)/Sata(0x0,0x0)/HD(1,MBR,0x7678D547,0x3F,0xFB03C1)
fs1 :Removable HardDisk - Alias hd19b0b0b blk1
PciRoot(0x0)/Pci(0x16,0x0)/USB(0x1,0x0)/USB(0x1,0x0)/HD(1,MBR,0x05A795F8,0x3F,0x7917C1)
blk0 :HardDisk - Alias hd21a65535a1 fs0
PciRoot(0x0)/Pci(0x18,0x0)/Sata(0x0,0x0)/HD(1,MBR,0x7678D547,0x3F,0xFB03C1)
blk1 :Removable HardDisk - Alias hd19b0b0b fs1
PciRoot(0x0)/Pci(0x16,0x0)/USB(0x1,0x0)/USB(0x1,0x0)/HD(1,MBR,0x05A795F8,0x3F,0x7917C1)
blk2 :BlockDevice - Alias (null)
PciRoot(0x0)/Pci(0x18,0x0)/Sata(0x0,0x0)
blk3 :Removable BlockDevice - Alias (null)
PciRoot(0x0)/Pci(0x16,0x0)/USB(0x1,0x0)/USB(0x1,0x0)
Press ESC in 3 seconds to skip startup.nsh, any other key to continue.
Shell>

Figure 36 - Indentify USB flash drive in EFI shell

8. Go to USB flash drive by typing **fs1:** followed by **ENTER**

```
Shell> fs1:
```

9. Go to the folder with the BIOS update utility and BIOS binary.
10. Type the command **AfuEfix64.efi filename.rom /p /b /n** to update the BIOS. (filename.rom is the BIOS file).

```
fs1:\Rangeley\BIOS> AfuEfix64.efi 0ACCN004_01.ROM /p /b /n
```

11. Wait for utility to complete. **DO NOT CYCLE POWER DURING UPDATE**.

```
 05/23/13  12:06p             6,291,456  0ACCN004_01.ROM
       10 File(s)  30,350,950 bytes
        2 Dir(s)


fs1:\Rangeley\BIOS> AfuEfix64.efi 0ACCN004_01.ROM /p /b /n
+-------------------------------------------------------------------------------+
|                AMI Firmware Update Utility  v3.04.02                          |
|      Copyright (C)2012 American Megatrends Inc. All Rights Reserved.          |
+-------------------------------------------------------------------------------+
 Reading flash ............... done
 - FFS checksums ......... ok
 Erasing Boot Block .......... done
 Updating Boot Block ......... done
 Verifying Boot Block ........ done
 Erasing Main Block .......... done
 Updating Main Block ......... done
 Verifying Main Block ........ done
 Erasing NVRAM Block ......... done
 Updating NVRAM Block ........ done
 Verifying NVRAM Block ....... done

fs1:\Rangeley\BIOS>
fs1:\Rangeley\BIOS> _
```

Figure 37 - BIOS Update Complete

12. Once update is complete, cycle power.

2.5 Updating Rangeley GbE EEPROM

1. Download the latest Intel Network Connection Tools from the Intel Business Portal (IBP) (Document #348742).
2. Copy the EFIx64 tools to a USB flash drive
3. Copy the Rangeley EEPROM update file to the USB flash drive. File should be in test format.
4. Insert USB flash drive into RCC system.
5. Power on RCC system
6. Press **ESC** when requested by the BIOS to enter the BIOS setup screen
7. Go to **Save & Exit** and under **Boot Override** select **UEFI: Built-in EFI Shell**

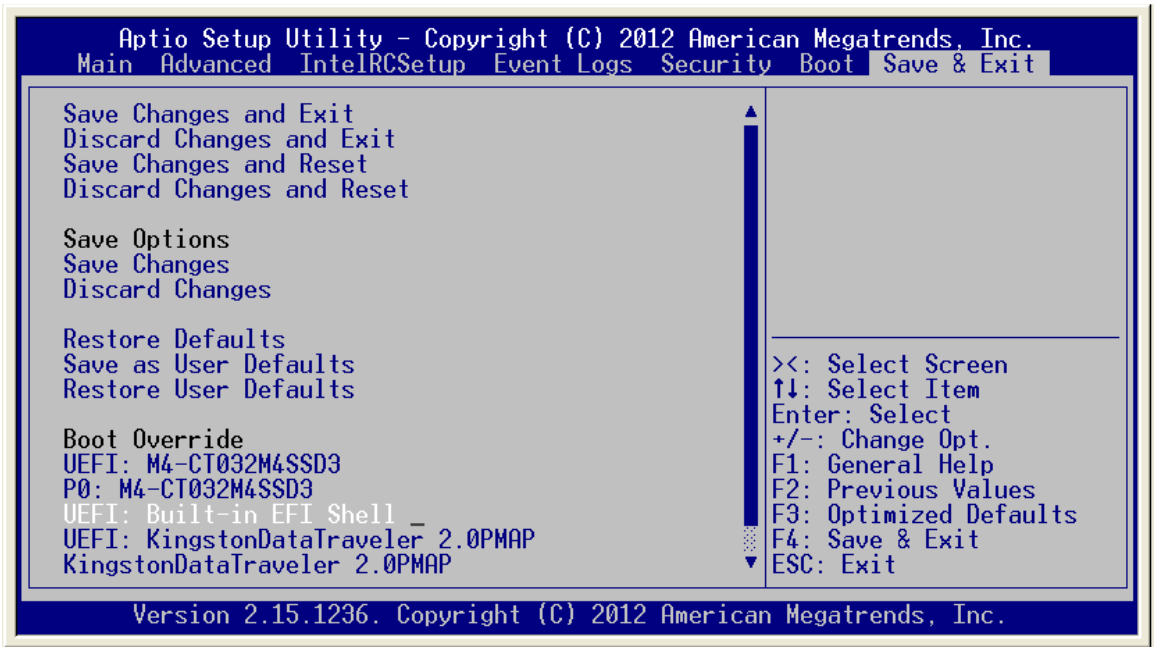

Figure 38 - BIOS, boot Built-in EFI Shell

8. USB flash drive will be identified as an **fs** device and labeled as a **Removable HardDisk**. In this example, the USB flash drive is fs1.

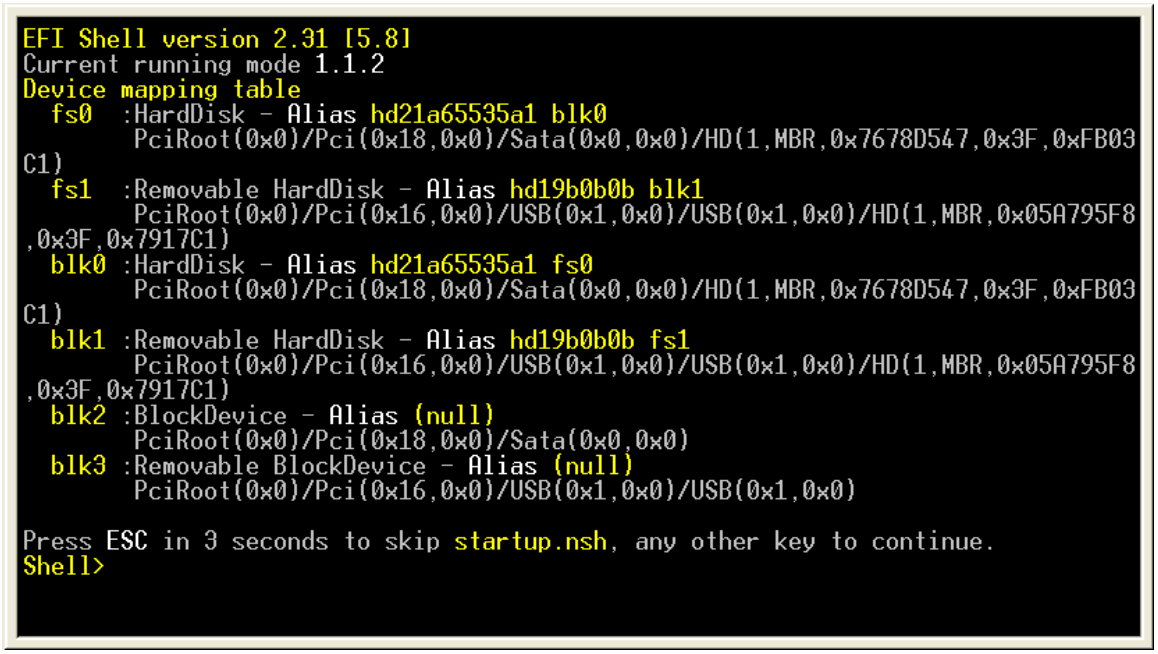
EFI Shell version 2.31 [5.8]
Current running mode 1.1.2
Device mapping table
fs0 :HardDisk - Alias hd21a65535a1 blk0
PciRoot(0x0)/Pci(0x18,0x0)/Sata(0x0,0x0)/HD(1,MBR,0x7678D547,0x3F,0xFB03C1)
fs1 :Removable HardDisk - Alias hd19b0b0b blk1
PciRoot(0x0)/Pci(0x16,0x0)/USB(0x1,0x0)/USB(0x1,0x0)/HD(1,MBR,0x05A795F8,0x3F,0x7917C1)
blk0 :HardDisk - Alias hd21a65535a1 fs0
PciRoot(0x0)/Pci(0x18,0x0)/Sata(0x0,0x0)/HD(1,MBR,0x7678D547,0x3F,0xFB03C1)
blk1 :Removable HardDisk - Alias hd19b0b0b fs1
PciRoot(0x0)/Pci(0x16,0x0)/USB(0x1,0x0)/USB(0x1,0x0)/HD(1,MBR,0x05A795F8,0x3F,0x7917C1)
blk2 :BlockDevice - Alias (null)
PciRoot(0x0)/Pci(0x18,0x0)/Sata(0x0,0x0)
blk3 :Removable BlockDevice - Alias (null)
PciRoot(0x0)/Pci(0x16,0x0)/USB(0x1,0x0)/USB(0x1,0x0)
Press ESC in 3 seconds to skip startup.nsh, any other key to continue.
Shell>

Figure 39 - Indentify USB flash drive in EFI shell

9. Go to USB flash drive by typing **fs1:** followed by **ENTER**

```
Shell> fs1:
```

10. Go to the folder with the eeupdate64e.efi update utility and EEPROM text file.
11. Type **eeupdate64e.efi** followed by **ENTER**

```
Using: Intel (R) PRO Network Connections SDK v2.21.1
EEUPDATE v5.21.01.03
Copyright (C) 1995 - 2013 by Intel (R) Corporation.
Intel (R) Confidential and not for general distribution.

Warning: No Adapter Selected

NIC Bus Dev Fun Vendor-Device  Branding string
=== === === === ============= ================================================
  1   3  00  00   8086-10FB    Intel(R) 82599 10 Gigabit Dual Port Network Conn
  2   3  00  01   8086-10FB    Intel(R) 82599 10 Gigabit Dual Port Network Conn
  3   0  20  00   8086-1F41    Intel(R) Ethernet Connection I354
  4   0  20  01   8086-1F41    Intel(R) Ethernet Connection I354
  5   0  20  02   8086-1F41    Intel(R) Ethernet Connection I354
  6   0  20  03   8086-1F41    Intel(R) Ethernet Connection I354


fs1:\Rangeley\1G> eeupdate64e.efi
```

Figure 40 - eeupdate64e.efi Adapter Identification

12. Rangeley ports are identified by Vendor-Device 8086-1F41. To update the Rangeley EEPROM, one of its NICs should be selected in the update command. Below is an example of the update command.

```
fs1:\Rangeley\1G> eeupdate64e.efi /nic=3 /d=ADI_RCC_Avn_4p_SGMII_NoMNG_16k.txt
```

13. Wait for command to complete and verify it reports successful. **DO NOT CYCLE POWER DURING UPDATE**.

2.6 Updating 82599 EEPROM

1. Follow steps 1 through 11 for updating Rangeley EEPROM
2. 82599 ports are identified by Vendor-Device 8086-10FB. To update the 82599 EEPROM, one of its NICs should be selected in the update command. Below is an example of the update command.

```
fs1:\Rangeley\10G> eeupdate64e.efi /nic=1 /d=82599_SFI_NO_MNG_4.25.txt
```

3. Wait for command to complete and verify it reports successful. **DO NOT CYCLE POWER DURING UPDATE**.

2.7 Updating Management FPGA

2.7.1 Updating FPGA over JTAG

The Management FPGA can be updated over JTAG. The tools required to update the FPGA over JTAG are below:

- Microsemi FlashPro4 programmer (http://www.microsemi.com/fpga-soc/design-resources/programming/flashpro#overview)
- Host computer with Windows OS and FlashPro software installed. (http://www.microsemi.com/fpga-soc/design-resources/programming/flashpro#downloads)
- FPGA bitfile. Provided from Intel and ADI in the form of .stp file.

Instructions:

1. Turn off power to RCC system.
2. Remove enclosure cover. Held on by two screws.
3. Connect FlashPro4 adapter to RCC system

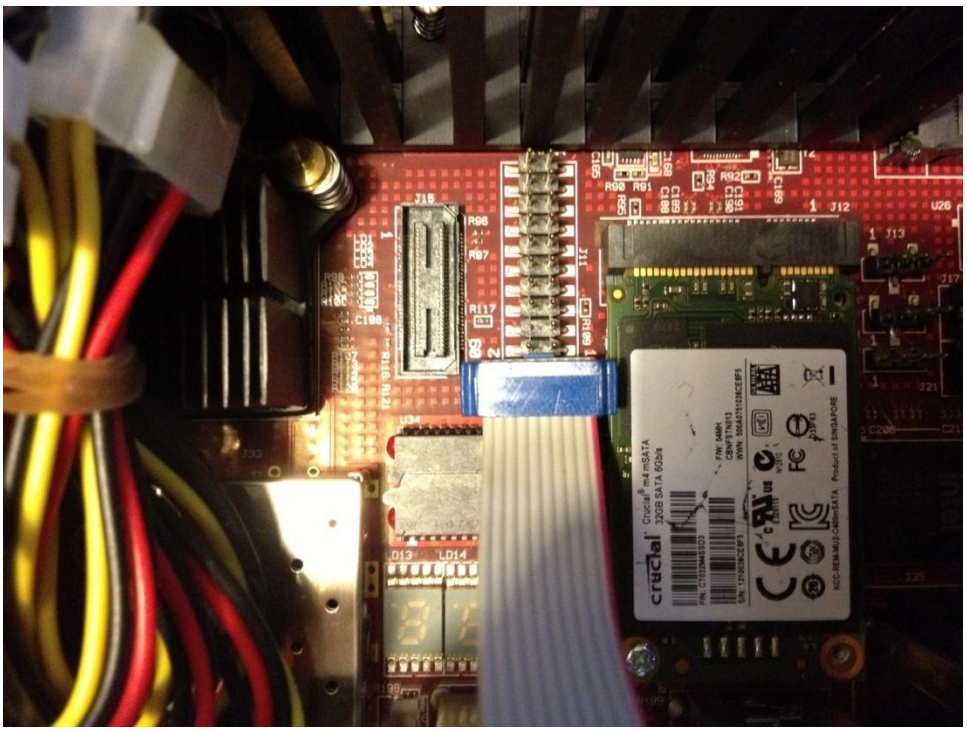

Figure 41 - Connect FlashPro4 Cable

4. Turn on power to RCC system

5. Open FlashPro program
6. Select **New Project** button

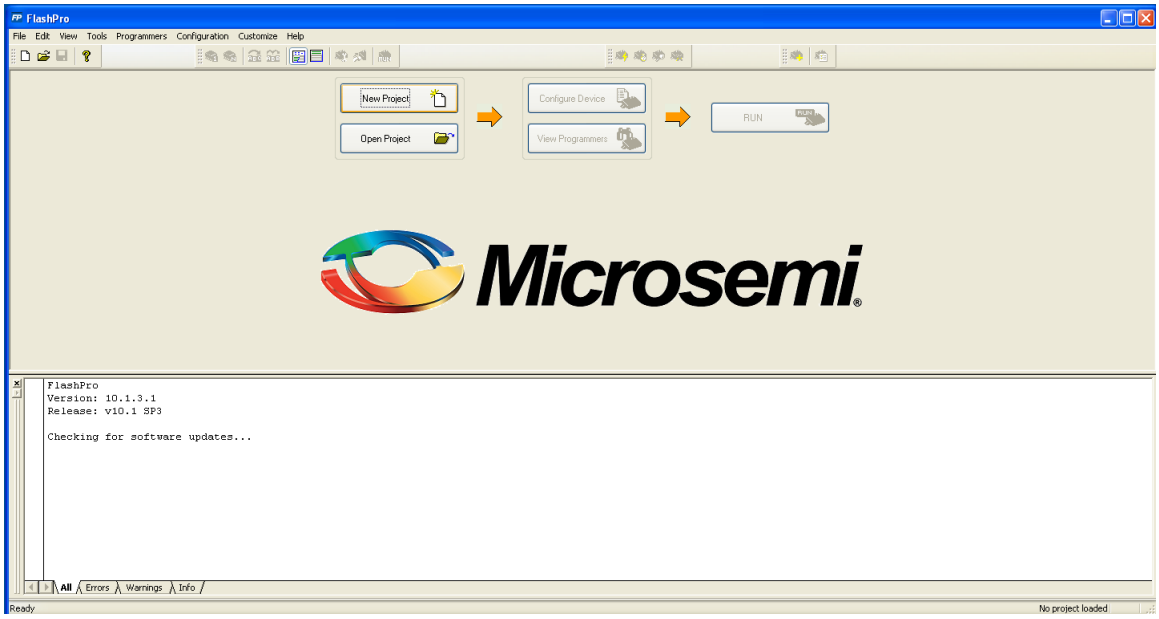

Figure 42 - FlashPro New Project

7. Enter name for new project and select location. **Single device** should be selected.

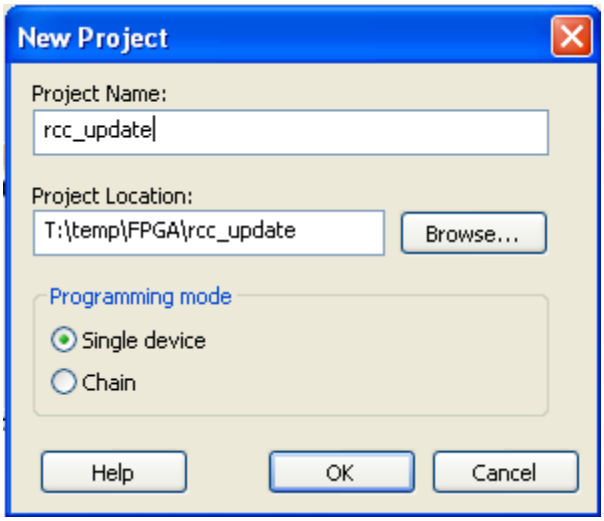

Figure 43 - FlashPro New Project Name

8. Select **Configuration->Load Programming File**

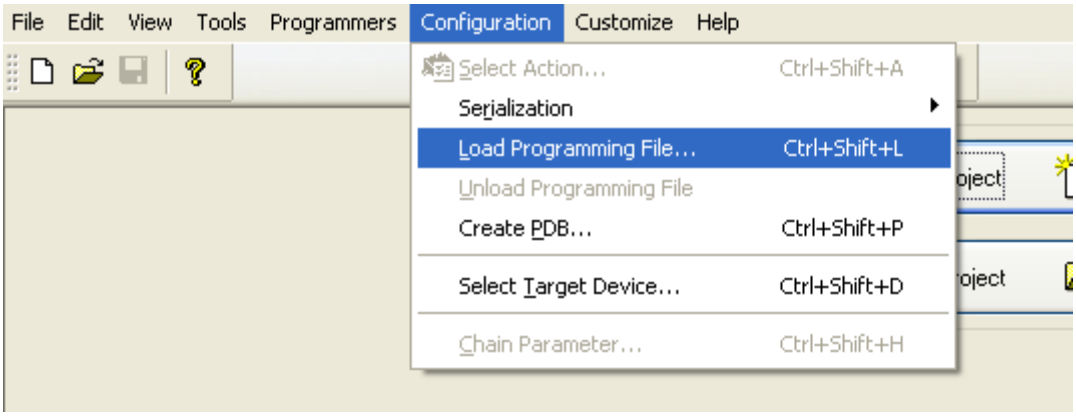

Figure 44 - FlashPro, Load Programming File

9. Select **PROGRAM** button.
10. Wait for program to Erase, Program, and then Verify update

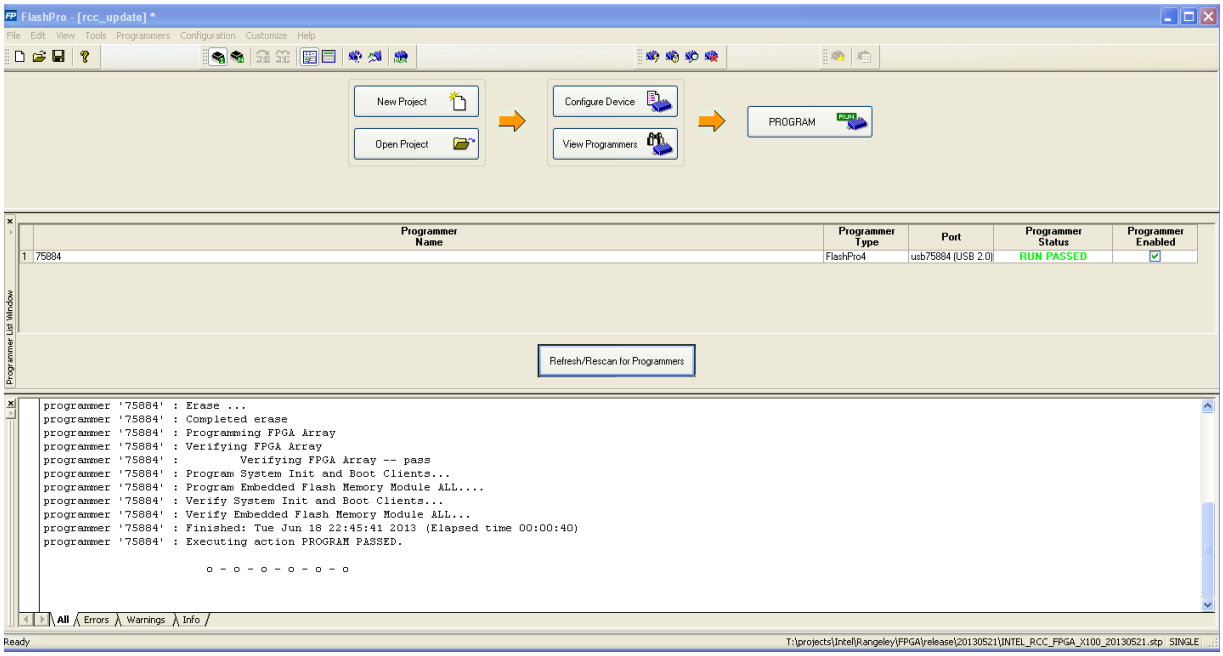
FlashPro - [rcc_update] *
New Project
Open Project
Configure Device
View Programmers
PROGRAM
Programmer Name
Programmer Type
Port
Programmer Status
Programmer Enabled
75884
FlashPro4
usb75884 (USB 2.0)
RUN PASSED
Refresh/Rescan for Programmers
programmer '75884' : Erase ...
programmer '75884' : Completed erase
programmer '75884' : Programming FPGA Array
programmer '75884' : Verifying FPGA Array
programmer '75884' : Verifying FPGA Array -- pass
programmer '75884' : Program System Init and Boot Clients...
programmer '75884' : Program Embedded Flash Memory Module ALL....
programmer '75884' : Verify System Init and Boot Clients...
programmer '75884' : Verify Embedded Flash Memory Module ALL...
programmer '75884' : Finished: Tue Jun 18 22:45:41 2013 (Elapsed time 00:00:40)
programmer '75884' : Executing action PROGRAM PASSED.
o - o - o - o - o - o - o
All Errors Warnings Info
Ready

Figure 45 - FlashPro FPGA Update Complete

11. Disconnect FlashPro4 programmer
12. Power cycle RCC system

2.7.2 Updating FPGA over console

This is a future feature not currently supported.

3 SUPPORT

Support related to the RCC system (i.e. Hardware, BIOS, Firmware, etc..) will be provided by ADI Engineering. Each kit comes with a standard support package which includes free technical support (up to 3 hours) from the engineering team and unlimited access to ADI's web-based support forums and download site.

Some customers may need extra support to handle hardware or software development tasks such as system-level design issues when integrating an ADI product into a larger system (thermal, regulatory, mechanical, etc.), software porting, debug or testing efforts, or design customization. Customers may also require design review or consulting services to quickly ramp up their engineering and manufacturing teams. For these customers ADI offers a variety of support packages to meet their specific requirements.

Support Package	Key Features	ADI Part Number
Standard Development Kit Support	• 90 day standard kit warranty • Unlimited access to ADI's web-based support site • Phone & Email Support during warranty and support period (3 business day response) • Up to 3 hours of support problem solving during the support period	DKSS
Premium Development Kit Support	• Extends product warranty and support period to 1 year • Unlimited access to ADI's web-based support site • Phone & Email Support during warranty and support period (1 business day response) • Up to 40 hours of support problem solving and hardware/software engineering assistance during the support period	DKPS-040
Hourly Support Packages	• Up to 8 hours of support problem solving and engineering assistance over 1 year	HSP-008
	• Up to 16 hours of support problem solving and engineering assistance over 1 year	HSP-016
	• Up to 40 hours of support problem solving and engineering assistance over 1 year	HSP-040
	• Up to 100 hours of support problem solving and engineering assistance over 1 year	HSP-100
	• Up to 400 hours of support problem solving and engineering assistance over 1 year	HSP-400
	• Up to 1000 hours of support problem solving and engineering assistance over 1 year	HSP-1000

Table 3 - ADI Support Plans

For questions related to the Intel SoC silicon, please contact your Intel representative.